



# **NAVAL POSTGRADUATE SCHOOL**

**MONTEREY, CALIFORNIA**

## **THESIS**

**OPTIMIZING MULTI-SHIP, MULTI-MISSION  
OPERATIONAL PLANNING FOR THE JOINT FORCE  
MARITIME COMPONENT COMMANDER**

by

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March 2009

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**OPTIMIZING MULTI-SHIP, MULTI-MISSION OPERATIONAL PLANNING  
FOR THE JOINT FORCE MARITIME COMPONENT COMMANDER**

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Submitted in partial fulfillment of the  
requirements for the degree of

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from the

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## ABSTRACT

Operational-level planners in Maritime Operations Centers aim to assign naval forces in support of combatant commanders efficiently and effectively, but they lack a software-based planning tool to develop optimal ship employment schedules. They must assign ships to particular missions spread throughout numerous regions over a particular time horizon to meet the combatant commander’s force requirements. Currently, this is a manual process. We present Navy Mission Planner (NMP), a decision aid based on an integer linear program that allows efficient generation of candidate employment schedules. NMP uses constrained, stack-based enumeration of candidate employment schedules over the feasible region. Total enumeration can produce an enormous number of schedules—easily reaching quadrillions of feasible solutions. By constraining the enumeration to eliminate impractical schedules, we can manage the computational burden and provide the naval planner useful solutions containing a near-optimal set of employment schedules for each assigned ship over the planning horizon. We submit a realistic scenario and provide a credible, face-valid solution to the multi-ship, multi-mission assignment problem, with sets of employment schedules that are as good as or better than sets produced manually.

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## **LIST OF ABBREVIATIONS AND ACRONYMS**

|          |  |
|----------|--|
| AD       | Air Defense                                  |
| ASW      | Antisubmarine Warfare                        |
| C3F      | Commander, U.S. Third Fleet                  |
| CFMCC    | Combined Forces Maritime Component Commander |
| CMC      | Concurrent Mission Capable                   |
| COCOM    | Combatant Command                            |
| CONOPS   | Concept of Operations                        |
| FFC      | Fleet Forces Command                         |
| GAMS     | General Algebraic Modeling System            |
| Intel    | Intelligence                                 |
| JFMCC    | Joint Force Maritime Component Commander     |
| JP       | Joint Publication                            |
| MCM      | Mine Countermeasures                         |
| MHQ      | Maritime Headquarters                        |
| MIO      | Maritime Interception Operations             |
| MOC      | Maritime Operations Center                   |
| NCC      | Naval Component Commander                    |
| NMP      | Navy Mission Planner                         |
| NSFS     | Naval Surface Fire Support                   |
| NWDC     | Navy Warfare Development Command             |
| NWP      | Navy Warfare Publication                     |
| OPCON    | Operational Control                          |
| PACFLT   | Commander, U.S. Pacific Fleet                |
| SubIntel | Submarine Intelligence Collection            |
| SUW      | Surface Warfare                              |
| TACMEMO  | Tactical Memorandum                          |
| TACON    | Tactical Control                             |
| TBMD     | Theater Ballistic Missile Defense            |
| VBA      | Visual Basic                                 |

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## **EXECUTIVE SUMMARY**

Maritime component commanders employ naval forces in support of the combatant commander. To support the commander's goals, staff planners in Maritime Operations Centers assign particular ships to particular missions in particular regions at particular times. In this era of limited resources, requirements often exceed resources, and the challenge for planners is to assign available resources efficiently and effectively. They currently lack a software-based planning tool to develop optimal ship employment schedules.

There are many factors involved in building a fleet schedule. Ships flow in and out of theater. Areas of operations typically cover large geographic areas. Some areas require multiple missions to meet the combatant commander's force requirements, and some missions require support from multiple units.

Currently, fleet scheduling is a manual process. Schedulers must juggle numerous requirements, and they typically do so with the help of a whiteboard and marker pens.

Navy Mission Planner (NMP) seeks to remove some of the complexity and reduce the time involved in mission planning and course of action development. NMP is a decision aid based on an integer linear program that takes the planner's inputs and returns a set of optimized ship employment schedules. The user inputs regions, or operating areas, and defines adjacency arcs connecting the regions. The planner then defines which missions are required on which days in which regions and assigns the value of each mission, thus setting the priorities in case requirements exceed resources. The planner also defines any prerequisite missions to be fully accomplished prior to the commencement of the desired mission. The user then notes the available ships, the days these ships are in theater, each ship's entry point into the area of operations, and set of concurrent mission capabilities (CMCs) available to that ship. CMCs define the ship's ability to complete multiple missions concurrently.

The NMP user interface is a Microsoft Excel spreadsheet. Excel, through Visual Basic code, enumerates candidate schedules for each ship. Because total enumeration can produce an enormous number of schedules—easily reaching quadrillions of feasible solutions, we limit the enumeration by defining the maximum number of schedules as well as a subset, the maximum number of schedules per ship. By constraining the enumeration process, we can provide the naval planner useful solutions containing the optimal set of employment schedules for each assigned ship over the planning horizon.

Excel sends the set of inputs to the General Algebraic Modeling System (GAMS). GAMS uses the commercial solver CPLEX to find the optimal set of ship employment schedules that maximizes the aggregate value of all maritime missions accomplished over the planning horizon.

NMP supports ever-changing scenarios and provides credible, face-valid solutions to the multi-ship, multi-mission assignment problem. NMP shifts the computational burden away from the operational planner and onto the computer. The CPLEX solver ensures that the sets of employment schedules are as good as or better than any set produced manually.

## ACKNOWLEDGMENTS

I dedicate this work to my beloved father. While he did not see the completion of this project, his memory remains to guide me through all that lies ahead.

Nothing I have done would be possible without the love and support of my family. I thank Tracie for putting up with me for fifteen years. Julianna and Andrew may not understand why we keep moving, but they love me anyway. My Mom has been a constant pillar of love and support my entire life. I love you all deeply and unconditionally.

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## **I. INTRODUCTION**

### **A. PURPOSE AND OVERVIEW**

The goal of military planning is to find the most effective means to reach a desired end state, as defined by the combatant commander. The commander may declare certain milestones from which to gauge success, such as the accomplishment of a certain set of missions. The operational planner must then turn the commander's guidance into an operation plan that specifies the forces, support, and resources required to accomplish the right missions to achieve the combatant commander's goals (JP 1-02, 2001). U.S. Navy Warfare Publication (NWP) 5-01 (2007) specifies a Navy planning process in which the planner identifies the end state and works to fill in the details, such as force employment and support, which will enable mission accomplishment.

United States Fleet Forces Command (FFC) requires a standardized level of planning and execution at the operational level of war. The Maritime Headquarters with Maritime Operations Center (MHQ with MOC) is the instrument through which the operational commander, typically the Combined or Joint Forces Maritime Component Commander (C/JFMCC), employs naval forces for the combatant commander. The MHQ with MOC concept applies to naval component commands, numbered fleets, and principal headquarters commands (FFC, 2007).

The operational commander employs naval forces to accomplish the military objectives of the joint force. Planners decide force allocation during the Concept of Operations (CONOPS) development phase of planning. NWP 5-01 relies on the skill and experience of commanders and planners to design campaigns and efficiently assign forces. The term for this design is "operational art."

Navy planners within the MOC cannot be certain that their practice of operational art results in optimal force employment. There is currently no multi-period operational planning tool able to assign an optimal mix of multiple assets to multiple missions over

multiple regions. Dugan (2007) provides an initial formulation of such a tool; this research continues Dugan's work and expands its capability to generate and evaluate operational plans.

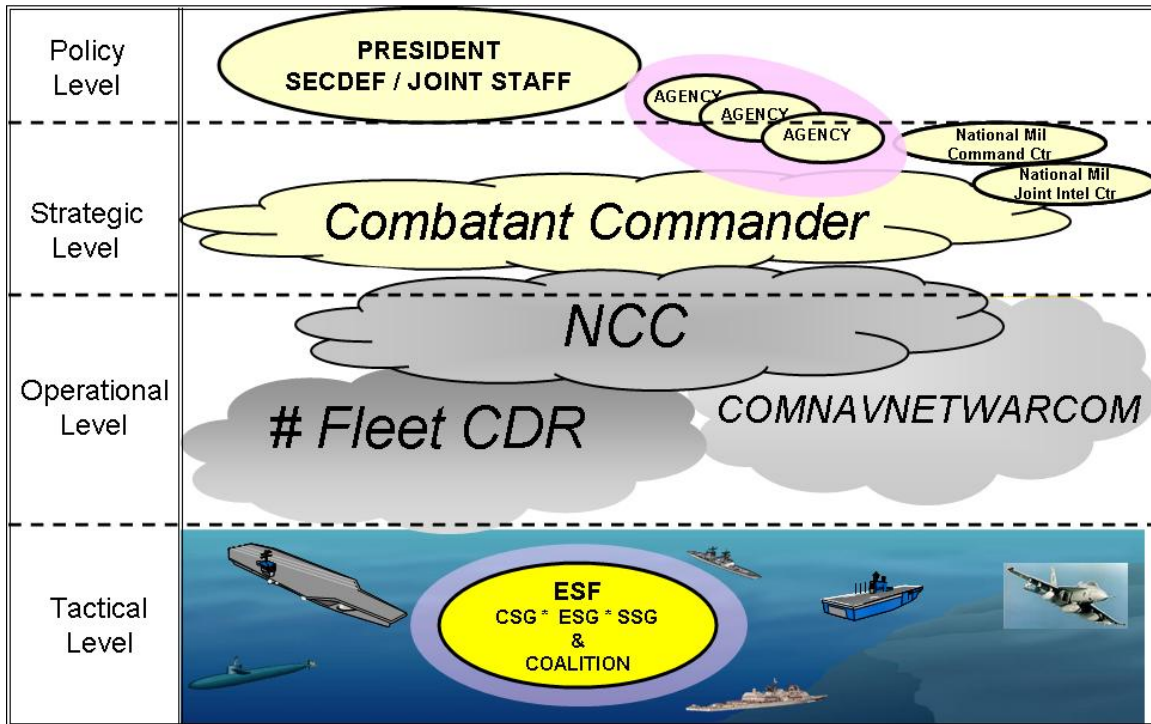
## **B. BACKGROUND**

### **1. Operational Level of War**

MOC planners are focused on the operational level of war, which concerns the planning and execution of major operations and campaigns in order to secure strategic objectives within a theater of operations (JP 1-02, 2001). It follows that the operational level planner must avoid a narrow or tactical point of view. The planner must consider the effects that naval force employment has on joint, combined, or interagency objectives (FFC, 2007).

Zvijac (2008) points out that planning, information, and relationships are critical at the operational level of war. Operational planners must focus on priorities and synchronization rather than on tactics. NWP 5-01 (2007) guides naval planners through this process.

While the operational commander plans and conducts major operations with strategic goals in mind (JP 1-02, 2001), the tactical units themselves actually perform the operations. Figure 1 depicts the relationship between the operational commander and the rest of the chain of command, from the policy level to the tactical level of command.



**Figure 1. Levels of Command.** The operational commander takes direction from the combatant commander at the strategic level of war and directs operations conducted by subordinate forces at the tactical level of war. The naval operational commander is usually the numbered fleet commander or naval component commander (NCC). The NCC, typically the C/JFMCC, touches the strategic level and must be familiar with the strategic goals of the combatant commander and plan operations conducive to accomplishing those goals (From: Slade, 2007).

## 2. Command and Control Organizational Design

Mission planning is a process through which the planner determines a course of action. The process begins by defining required tasks, assigning resources to accomplish those tasks, and implementing a timeline for completing the tasks (Levchuk et al., 2002). Given the complex nature of planning military operations with limited resources, assigning the optimal mix of forces to the right regions in the theater of operations at the right times is a difficult task.

Levchuk et al., (2002) describe a method to model large organizations and devise mission planning strategies. They seek to achieve an optimal solution to meet mission goals and use resources efficiently. In the context of their research, mission planning

means building the structure of the organization to use its human resources and meet the organization's goals. Their concepts are easily extended to military mission planning—the efficient use of military assets to accomplish the commander's tasking.

Levchuk et al., (2002) present a mathematical model to solve the allocation problem. Their interest as organizational designers is to minimize total mission completion time, i.e., the time to complete all tasks required for the mission. Naval operational planners instead seek to maximize mission accomplishment. Levchuk et al.'s concepts are germane, but their mathematical formulation solves a different problem than the force allocation problem facing the operational commander. Levchuk et al., assign a task (mission) to a platform (ship) and specify a start time (start day). A platform does not perform multiple tasks simultaneously, and task requirements do not change day-by-day. The naval planner needs a multiple period, multiple mission operational model to prioritize and schedule missions, regions, and times.

### **3. Navy Mission Planner**

Dugan (2007) begins development of Navy Mission Planner (NMP), a decision aid to help the C/JFMCC assign forces and missions. NMP is Microsoft Excel-based and exports data to the General Algebraic Modeling System (GAMS, 2009) using the commercial solver CPLEX (2009), to solve the commander's problem. The version of NMP presented here consists of an Excel spreadsheet and Visual Basic macros that store and process scenario data, and an integer linear programming model written in the GAMS algebraic modeling language.

The user interface is an Excel workbook that accepts all user inputs, creates data files in the appropriate format for the GAMS model, and runs GAMS/CPLEX to find the best set of employment schedules for the available assets. The output is a text file containing the optimal ship employment schedules as well as any gaps in mission completions.



Dugan’s notional scenario comprises 11 ships and 65 missions in 24 regions. We expand the scenario size to include 18 ships and 80 missions, excluding the aircraft carrier and its escort cruiser, which typically operate independently and support tasking from the Joint Forces Air Component Commander.

### **C. SCOPE AND OBJECTIVES**

The goal of this research is to expand the functionality of NMP and provide a useful tool to the JFMCC planning staff. Dugan’s (2007) formulation remains the backbone of NMP; however, the biggest limitation of that is the very small list of possible employment schedules per ship (~5 schedules per ship). We develop a new version of the NMP integer programming model to encompass more employment schedules through constrained enumeration of the feasible region. Total enumeration can produce an unwieldy number of schedules—easily reaching quadrillions of feasible solutions. By constraining the enumeration to eliminate impractical schedules, we significantly reduce the computational burden and still provide useful solutions to the naval planner. We modify the interface and model to handle tens of thousands of employment schedules per ship, leading to much better overall solutions and a much more flexible operational planning tool.

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## **II. MARITIME MISSION SUPPORT**

### **A. MHQ WITH MOC**

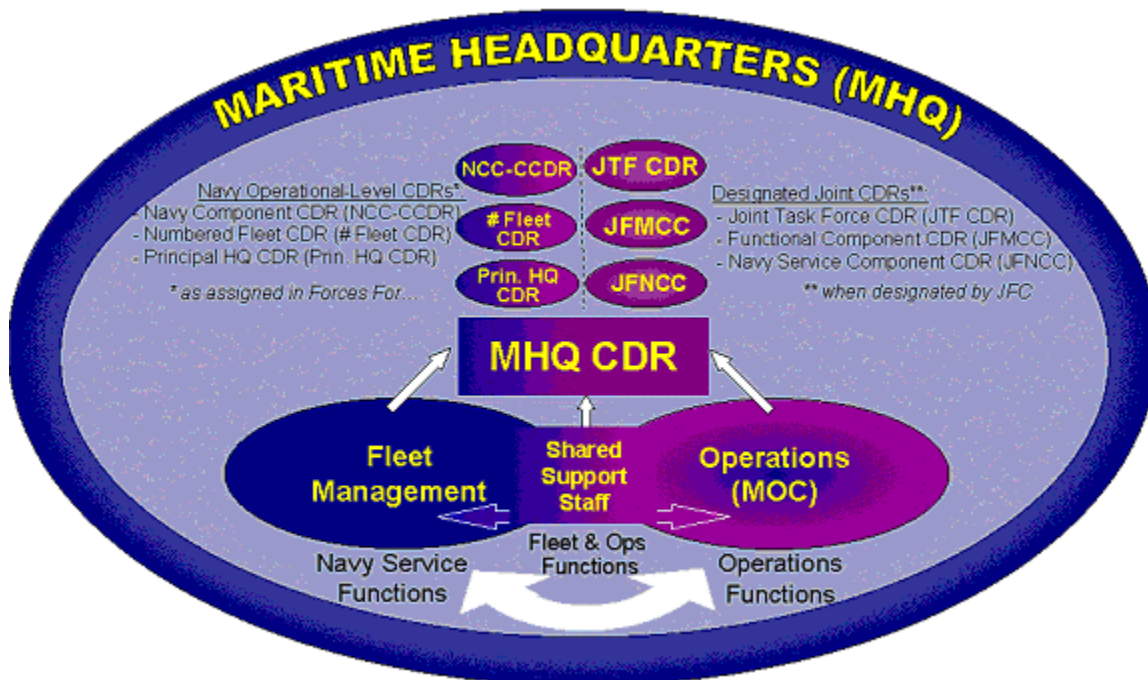
#### **1. Introduction**

FFC (2007) describes MHQ with MOC as a “rapidly deployable globally networked headquarters.” It develops MHQ with MOC because of lessons learned in Operation Enduring Freedom and Operation Iraqi Freedom. Naval operational commands lag behind other services in command and control capabilities and joint planning experience. MHQ with MOC serves to close the gap by standardizing naval operational level commands, properly training and educating personnel, and networking all fleet headquarters commands.

#### **2. MHQ Functional Description**

Title 10 United States Code directs the services to man, train, and equip their forces. Operational level naval commands perform these fleet management roles to varying degrees in addition to conducting operations. The MHQ supports both fleet management and operational duties “across the full range of military operations and throughout the maritime environment” (FFC, 2006).

The current MHQ organizes its staff into three functional categories pictured in Figure 2. Dedicated staff elements perform fleet management functions, while personnel assigned to the MOC direct naval and joint maritime operations. The third element of the MHQ is a support staff shared by the fleet management staff and MOC staff. The support staff typically performs administrative, legal, and medical functions (FFC, 2007).



**Figure 2. MHQ with MOC Organization.** Navy Mission Planner is a planning tool for the operational planner in the Maritime Operations Center. Figure 2 shows the relationship of the MOC within the Maritime Headquarters. MOC is one of three main elements of the MHQ. The others are the fleet management division and support staff. The figure also captures the dual-hat nature of the MHQ commander as a navy operational commander and a joint component commander (From: FFC, 2007).

### 3. MOC Functions

The MOC is a complex organization and includes all personnel and equipment that support the conduct of naval and joint operations. The MOC organization conforms to the Navy standard staff organization of boards, centers, bureaus, cells, working groups, and teams. The MOC “assess[es], plan[s], and execute[s] operational level missions, including strategic communications, theater security cooperation, intelligence preparation of the environment, and maritime security operations” (FFC, 2007). MOC takes on numerous roles to accomplish these missions. In addition to directing operations, the MOC establishes a chain of command for and delegates command authority to subordinate commanders.

#### **4. Operational Control**

Navy Warfare Development Command TACMEMO 3-32-06, Combined/Joint Force Maritime Component Commander (C/JFMCC) Planning and Execution (NWDC, 2006) provides guidance to operational commanders. NWDC (2006) defines operational control (OPCON) as:

command authority exercised by commanders at any echelon at or below the level of COCOM [combatant command] and can be delegated. OPCON is inherent in COCOM and is the authority to perform those functions of command over subordinate forces involving organizing and employing commands and forces, assigning tasks, designating objectives, and giving authoritative direction necessary to accomplish the mission.

The combatant commander usually delegates OPCON to the operational commander. OPCON differs from tactical control (TACON) in that TACON is short-term local direction specific to an assigned task or mission. While the MHQ normally retains OPCON, it typically delegates TACON to subordinate commanders.

#### **5. Planning in MHQ with MOC**

The Future Plans cell is responsible for developing long-term plans and orders. Future Operations takes responsibility for these plans as the time for execution grows nearer. The Future Operations cell sets mission priorities and allocates available forces to the missions (FFC, 2007).

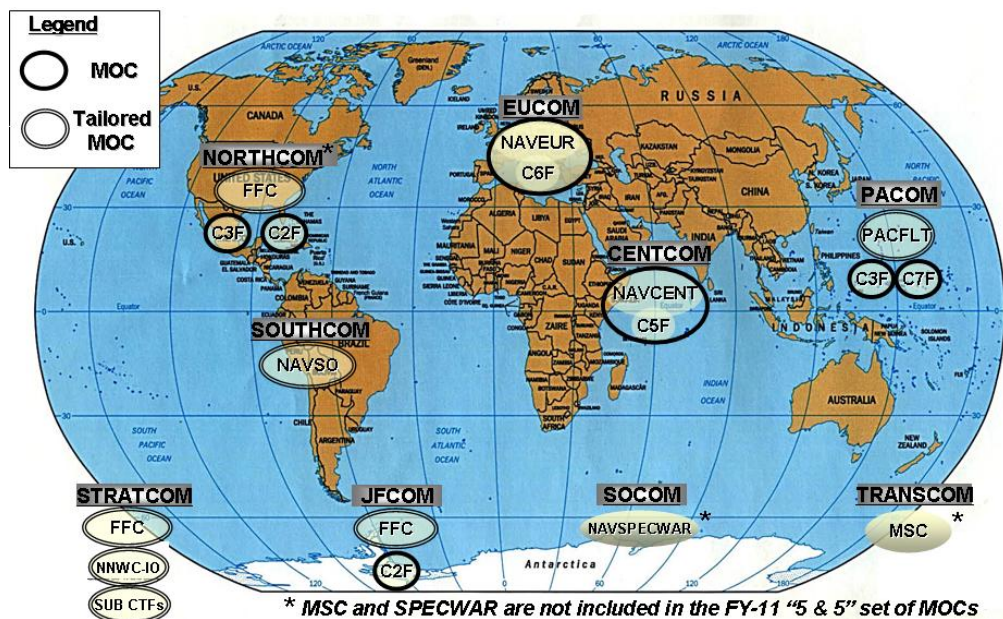
NWP 5-01 (2007) lists a detailed series of actions known as the Navy planning process in which the Future Plans and Future Operations cells produce the operation plans and orders. The process includes mission analysis, friendly and enemy course of action development, wargaming the options, and preparing the operation order. During course of action development, the operational planners complete worksheets, provided in NWP 5-01, to sketch out all aspects of the plan, to include force allocation.

The task of completing the NWP worksheets, i.e., assigning missions to forces in specific regions at specific times, is a manual process. Commander, U.S. Third Fleet Plans Directorate, specifically the Time-Phased Force Deployment Data and Joint Operation Planning and Execution System cell (Sironi, 2009), confirms this process.

Whiteboards and spreadsheets can assist the process of completing the worksheets, but planners manually insert forces to fill requirements. As requirements change, the planners rearrange their allocations.

There is no planning tool with an algorithm to optimize ship employment schedules. Some planning aids pull data from various sources to improve the display of information needed to craft the schedules (Sironi, 2009). According to Future Schedules Officers from the Third Fleet Operations Directorate (Baecker, 2009), other tools ensure that the ships in theater meet COCOM capability and presence requirements while observing the Chief of Naval Operations standards for operations tempo. None of the tools produce an optimal employment schedule by ship, mission, region, and day.

Figure 3 shows current MHQs under their respective combatant commanders. Note that in the current configuration, Military Sealift Command and Naval Special Warfare Command are MHQs without a MOC.



**Figure 3. U.S. MHQ and MOC Commands.** U.S. Fleet Forces Command considers the Navy component commanders, force commanders, and joint force maritime component commanders to be Maritime Headquarters. Each contains a Maritime Operations Center. Some MOC responsibilities vary according to requirements in the area of operations. These are tailored MOCs. For example, Commander, U.S. Pacific Fleet (PACFLT) is a tailored MOC, but Commander, U.S. Third Fleet (C3F) is a standard MOC (From: Slade, 2007).

## **B. FLEET FORCES COMMAND VISION FOR MHQ WITH MOC**

### **1. End State**

The U.S. Navy intends to be more than just a force-provider. FFC (2007) envisions a MHQ with MOC built for centralized command, distributed planning, and decentralized execution. Naval staffs have tended to take tactical views of operations, but MOC planners take operational views. The result is a MHQ fulfilling the role of a true operational commander providing full support to joint operations worldwide.

### **2. Transformation**

Full implementation of MOC requires change within the operational level staffs. FFC (2007) notes that naval staffs must further integrate into the joint planning process, standardize staff functions, ensure joint professional education for personnel, implement a certification and training process, and improve the staff planning process. Further, MHQs without a MOC operate mainly to provide fleet management functions. These MHQs treat operations functions as collateral duties.

The non-MOC MHQ staffs are challenged to efficiently shift roles between fleet management and operational duties. MOC provides a common organization dedicated to the operational role. Full implementation of an independent but linked MOC ensures greater staff efficiency, especially as operational commitments increase without a reduction in fleet management requirements (FFC, 2006).

NMP stands to facilitate the improvement of the MOC planning process. Dugan (2007) notes that assigning assets to missions and regions over the planning horizon is “time consuming and difficult.” NMP provides value to the MOC staff and allows for improving the staff planning process. NMP provides tens of thousands of courses of action, evaluates each one, and recommends the best solution by maximizing the value of assigned missions to create an optimal force mix.

Chapter III develops full NMP model specifications and inputs.

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### III. NMP OPTIMIZED MODEL WITH ENUMERATION

#### A. DESCRIPTION

NMP uses an integer linear program to compute the optimal employment schedule for each U.S. Navy combatant ship assigned to a particular area of operations. This research updates Dugan's (2007) original formulation and adds automatic schedule generation capability. The operational planner's inputs to NMP remain largely unchanged; therefore, the following discussion relies heavily on Dugan's original description.

The planner's initial NMP input is the set of *days* covering a finite planning horizon. The user then inputs the planned operating areas into NMP as *regions*, each of which is an area of the ocean specified by a latitude and longitude at or near its center. We modify Dugan's (2007) concept of a set of regions from a grid of rectangular regions to a connected network of nodes. The node concept provides the planner with flexibility to input desired areas of operation and to easily determine the shortest travel times between regions. (Note that the definition of a region does not restrict a ship to operating on one point in the water; individual units are free to maneuver as necessary around the region to accomplish the assigned mission.)

The user then defines adjacency *arcs*, representing unobstructed great-circle navigation routes between pairs of regions. NMP then computes and stores the arc lengths (in nautical miles), the shortest path between all regions in nautical miles using sequences of great circle arcs, and transit days (at 16 knots) required for each such path.

Mission requirements are specified in a list of *missions*, each of which has a *mission type*, drawn from a fixed list of types (e.g., air defense, surface warfare, etc., as defined in Chapter IV), a region, and a set of days for which it is required. In addition to the type, region, and day requirements, the planner defines, for each mission, in each region, on each day, a *value* for accomplishing that mission, and a set of *mission dependencies*, which define prerequisite missions that must be accomplished simultaneously with that mission, to enable other ships to complete it.

The last input set is the set of available *ships*. The operational planner defines the set of ships by hull number and name, start day, start region, and available *concurrent mission capability sets (CMCs)*. The start day is the first day of the planning horizon during which a ship is able to complete mission tasking. A single CMC set is a vector of *accomplishment* values, one for each mission type, that indicate the fraction of a particular mission that a ship can accomplish concurrently with other missions in the CMC set. One ship can have multiple CMC sets to choose from, but it can only operate under one CMC on any given day. Values less than one indicate reductions in readiness for various issues, such as maintenance or personnel.

The output from NMP is a set of *employment schedules*. Each ship's employment schedule specifies, for each day in the planning horizon, the region in which the ship operates and the assigned CMC set for that ship on that day in that region. NMP provides employment schedules to maximize the aggregate value of all maritime missions accomplished over the planning horizon (Dugan, 2007).

## **B. LIMITATIONS AND ASSUMPTIONS**

NMP limits the planning horizon to fifteen day windows due to operational limitations on ship employment schedules. One can model a full campaign by solving for a series of fifteen day windows using a “rolling horizon” approach.

NMP calculates transit time based on a 16-knot speed of advance and rounds fractional transit time to represent whole days. NMP rounds days down when the fractional element is less than eight hours. It rounds up when the fraction is greater than or equal to eight hours. In other words, NMP assumes that a unit may participate in missions if it arrives on station with at least two-thirds of a day remaining.

## **C. NMP INTEGER PROGRAM FORMULATION**

Many of the inputs to NMP are unchanged, but this research significantly changes the formulation of model. The following integer linear program solves for the optimal set of Navy ship employment schedules.

## 1. Sets and Indices [cardinality]

|                         |  |
|-------------------------|--|
| $s \in S$               | Ship (hull number and name, alias $s'$ ) [~50]   |
| $m \in M$               | Mission type (alias $m'$ ) [~10]<br>(e.g., AD, MIO, Intel, TBMD)   |
| $c \in C_s$             | Concurrent mission capability set for ship $s$ [~10]   |
| $m \in M_c$             | Mission types in concurrent (simultaneous) mission set $c$<br>(e.g., ship $s$ can simultaneously perform mission type $m$ in<br>concurrent mission capability set $c$ .)           |
| $p \in P$               | Employment schedules [~1 million]  |
| $p \in P_s \subseteq P$ | Employment schedules for ship $s$ [~1 million]<br><br>( $\bigcup_s P_s \equiv P$ , $P_s$ is a partition of $P$ .)  |
| $s(p)$                  | Ship of employment schedule $p$  |
| $r \in R$               | Regions in AOR [~30]   |
| $d \in D$               | Days in planning horizon (alias $d'$ , $d''$ ) [~14]   |
| $r(p, d)$               | Region employment schedule $p$ visits on day $d$   |
| $n \in N$               | Ordinal for multiple missions of the same mission type [~5]<br>(E.g., several ships may conduct ASW at the same time<br>within the same region, but with different effectiveness.) |

## 2. Data [units]

|                   |  |
|-------------------|--|
| $value_{m,n,r,d}$ | Priority of $n$ -th mission of type $m$ , in region $r$ on day $d$ [1-20]<br><br>[value]<br><br>( $\{m, n, r, d\} \in MNRD$ tuples exist only for non-zero values) |
|-------------------|--|

$accomplish_{c,m}$  Level of accomplishment of concurrent mission set  $c \in C_s$ ,

mission  $m \in M_c$  [0.0-1.0] (Note that each ship may have its own set of concurrent mission capability sets, and that some of these sets may contain the same missions, but with different accomplish rates to represent the ship choosing to change emphasis between missions.)

### 3. Induced Index Sets

$\{m, n, r, d\} \in MNRD$  4-tuple exists only if  $value_{m,n,r,d} > 0$  or  $accomplish_{s,m} > 0$  for

some ship that can employ a concurrent mission capability set that includes mission  $m$  in region  $r$  on day  $d$

$\{m, r, d\} \in MRD$  3-tuple exists only if  $\{m, n, r, d\} \in MNRD$  does for some  $n$

$\{m, r, d, m'\} \in MRDM$  4-tuple exists if, in region  $r$  on day  $d$ , mission  $m$  can be undertaken only if mission  $m'$  is fully accomplished

### 4. Variables [units]

$U_{m,n,r,d}$  Level of accomplishment of the  $n$ -th mission type  $m$  assignment in region  $r$  on day  $d$  [0.0-1.0]

$V_{m,r,d}$  =1 if mission  $m$  is fully accomplished in region  $r$  on day  $d$  [binary]

$W_{s,c,d,r}$  =1 if ship  $s$  employs concurrent mission capability  $c$  on day  $d$  in region  $r$  [binary]

$X_{s,s',r,d}$  =1 only if ships  $s$  and  $s'$  are both in region  $r$  on day  $d$  [binary]

$Y_p$  =1 if schedule  $p$  is selected [binary]

### 5. Formulation

$$\max \sum_{\{m,n,r,d\} \in MNRD} value_{m,n,r,d} U_{m,n,r,d} \quad (T0)$$

$$\text{s.t.} \quad \sum_{p \in P_s} Y_p = 1 \quad \forall s \in S \quad (\text{T1})$$

$$\sum_{c \in C_s} W_{s,c,d,r} \leq \sum_{\substack{p \in P_s \\ \wedge \exists r(p,d)}} Y_p \quad \forall s \in CS, d \in D, r \in R \quad (\text{T2})$$

$$\sum_{n|\{m,n,r,d\} \in MNRD} U_{m,n,r,d} \leq \sum_{s,c \in C_s} accomplish_{c,m} W_{s,c,d,r} \quad \forall \{m,r,d\} \in MRD \quad (\text{T3})$$

$$V_{m,r,d} \leq \sum_{\substack{p \in P || r=r(p,d) \\ \wedge c \in C_s(p) \wedge m \in M_c}} accomplish_{c,m} Y_p \quad \forall \{m,r,d\} \in MRD \quad (\text{T4})$$

$$V_{m,r,d} \leq \sum_{n|\{m,n,r,d\} \in MNRD} U_{m,n,r,d} \quad \forall \{m,r,d\} \in MRD \quad (\text{T4a})$$

$$U_{m,n,r,d} \leq V_{m',r,d} \quad \forall m,n,r,d | \{m,n,r,d\} \in MNRD \\ \wedge \{m,r,d,m'\} \in MRDM \quad (\text{T5})$$

$$U_{m,n,r,d} \in [0,1] \quad \forall \{m,n,r,d\} \in MNRD$$

$$V_{m,r,d} \in \{0,1\} \quad \forall \{m,r,d\} \in MRD$$

$$W_{s,c,d,r} \in \{0,1\} \quad \forall s \in S, c \in C_s, d \in D, r \in R$$

$$Y_p \in \{0,1\} \quad \forall p \in P \quad (\text{T6})$$

## 6. Discussion

The objective (T0) sums the total value of completed and partially completed missions. Each packing constraint (T1) allows exactly one employment schedule per ship. Each constraint (T2) permits a combatant to employ a concurrent mission capability on a given day only if an employment schedule exists for that ship. Each constraint (T3) limits the sum of the partial completion values of all missions by the total mission accomplishment for every tuple of mission, region, and day. Each constraint (T4) assigns full accomplishment to a mission in a particular region on a particular day only if there is at least one total unit of accomplishment for that same combination of

mission, region, and day. Similarly, each constraint (T4a) assigns full accomplishment to a mission in a particular region on a particular day only if each mission copy combines in that region on that day to produce at least one total unit of accomplishment. Constraints T4 and T4a are equivalent for determining optimal employment schedules,  $Y$ , but T4a enforces additional structure on the individual mission accomplishment variables,  $U$ , for prerequisite missions that have no prescribed value. Each constraint (T5) ensures that no mission accrues accomplishment in a given region on a given day unless each of its prerequisite missions (if any) in that region on that day has full accomplishment. (T6) defines the variable domains.

## **D. CONSTRAINED ENUMERATION**

### **1. General**

NMP builds candidate employment schedules, i.e., the values for  $r(p, d)$  for all  $p$  and  $d$ , through constrained enumeration. Total enumeration of all possible ship positions over each day in the planning horizon runs in exponential time and could produce an enormous number (e.g., for just ten regions over fifteen days, we have on the order of  $10^{15}$  feasible schedules per ship) of schedules. This result is impractical for many reasons, including unacceptably long runtime and system memory limitations. NMP limits the enumeration of schedules through various user-defined parameters.

Our implementation of a path enumeration algorithm avoids recursive programming by explicitly maintaining a stack of regions comprising a current partial path, and arrays that hold path data during the enumeration computations. The stack provides memory for the nodes on the current path. The top node on the stack becomes the source node for the enumeration of the remaining path completions. The arrays hold data for the positions of nodes on the current path, the forward-star structure, the list of outbound arcs from the node, and the next candidate arc in the forward-star (Carlyle, 2008).

## 2. Path Enumeration in NMP

Path enumeration in NMP begins by reading the user-defined limits on the number of ship schedules, *max schedules* and *max schedules per ship*, and the number of stall days, *max stall days per ship*. A stall day is a day in which a ship remains in the same region it occupied the previous day. The parameter *max schedules* is the main limit. When the number of schedules reaches this constraint, the enumeration terminates. Reducing the maximum allowable stall days permits NMP to consider a more diverse set of schedules within the number of maximum schedules. Conversely, increasing maximum stall days reduces diversity, but allows a single ship to stay on one long mission without rotating out.

This algorithm uses two stacks and six arrays. One stack (the region stack) holds incumbent path nodes, and the other (the next-region stack) points to candidate nodes. The arrays hold more data useful to the enumeration process. One flags each ship having a complete schedule. Two maintain ship employment schedules—one maintains daily resolution on covered regions and the other maintains regional assignments by ship. The fourth and fifth arrays store the start day and start region, respectively, for each ship. The last array counts the consecutive stationary days within a candidate schedule. This array ensures compliance with the constraint max stall days.

NMP treats the set of regions as a network, with user-defined arcs connecting the nodes (the regions themselves) along great-circle navigable routes. The source node is the planner input *start region*. NMP reads and stores the distances between regions, transforms the distances into transit days, and creates a new array to store this information.

With these administrative processes complete, NMP begins the actual task of building feasible schedules. The process entails a series of loops. The outer loop iterates through the list of ships.

Within the main outer loop, the second loop occurs while three conditions are true. The stack pointer, i.e., the current day of the incumbent schedule, must be greater

than or equal to the ship's start day. The second and third continuation conditions are that the number of schedules generated meets the constraints on total schedules generated and schedules generated per ship.

A third loop then begins and performs a depth-first search of remaining regions while the number of schedules generated meets the two schedule constraints. NMP considers all other nodes as candidates for the path until the last day of the planning horizon. NMP then starts building all possible directed paths, thought of as one way routes between regions, from source to sink by building a series of partial paths. At the end of an incumbent path, NMP enumerates all remaining completions of the path.

NMP considers leaving the ship in the current region if the ship has stall days remaining. If not, then NMP looks to the next region for a suitable mission for the given ship. If there is a feasible mission, then NMP adds the region to the next region stack.

Next, NMP compares the distance between the current and next regions. If the distance does not allow for transit in a single day, then the ship is unavailable until completion of the transit period.

At the final day of the planning horizon, NMP reaches the end of the depth-first search. It continues the enumeration loop until it has built every feasible schedule or has reached the maximum number of schedules.



## IV. ANALYSIS OF RESULTS

### A. SCENARIO

#### 1. Mission Types

Dugan (2007) applies ten mission types and two supporting mission types in NMP. We modify the NMP mission set to include eleven mission types and delete the supporting mission types Transit and Off-Station. NMP handles transit and off-station time within the underlying VBA code.

While representative of the most common maritime missions, our list of mission types is not intended to be exhaustive. The operational planner may define any mission type necessary to suit the commander's objectives. NMP accepts any mission name on the *Missions* worksheet.

Acronyms or abbreviations in parenthesis denote NMP notation. Joint Publication 1-02 (2001) defines the following, except as otherwise noted:

#### *a. Air Defense (AD)*

Defensive measures designed to destroy attacking enemy aircraft or missiles in the atmosphere, or to nullify or reduce the effectiveness of such attack. (JP 1-02, 2001)

We consider air defense separately from missile defense.

#### *b. Theater Ballistic Missile Defense (TBMD)*

A ballistic missile is:

any missile which does not rely upon aerodynamic surfaces to produce lift and consequently follows a ballistic trajectory when thrust is terminated. (JP 1-02, 2001)

Missile defense is:

defensive measures designed to destroy attacking enemy missiles, or to nullify or reduce the effectiveness of such attack. (JP 1-02, 2001)

We use the term TBMD to describe the naval mission of providing ballistic missile defense to a theater of operations.

***c. Antisubmarine Warfare (ASW)***

Operations conducted with the intention of denying the enemy the effective use of submarines. (JP 1-02, 2001)

***d. Surface Warfare (SUW)***

That portion of maritime warfare in which operations are conducted to destroy or neutralize enemy naval surface forces and merchant vessels. (JP 1-02, 2001)

***e. Strike***

An attack to damage or destroy an objective or a capability. (JP 1-02, 2001)

Naval fire resources are sea based or sea supported, and include Navy and Marine Corps lethal and nonlethal air-delivered weapons, maritime-based gunfire and land-attack missiles, and maritime-based naval special warfare units. (NWP 3-09.1, 2005)

***f. Naval Surface Fire Support (NSFS)***

Fire provided by Navy surface gun and missile systems in support of a unit or units. (JP 1-02, 2001)

***g. Maritime Interception Operations (MIO)***

Efforts to monitor, query, and board merchant vessels in international waters to enforce sanctions against other nations such as those in support of United Nations Security Council Resolutions and/or prevent the transport of restricted goods. (JP 1-02, 2001)

***h. Mine Countermeasures (MCM)***

All methods for preventing or reducing damage or danger from mines. (JP 1-02, 2001)

***i. Mine Warfare (Mine)***

The strategic, operational, and tactical use of mines and mine countermeasures. Mine warfare is divided into two basic subdivisions: the laying of mines to degrade the enemy's capabilities to wage land, air, and

maritime warfare; and the countering of enemy-laid mines to permit friendly maneuver or use of selected land or sea areas. (JP 1-02, 2001)

*j. Intelligence Collection (Intel)*

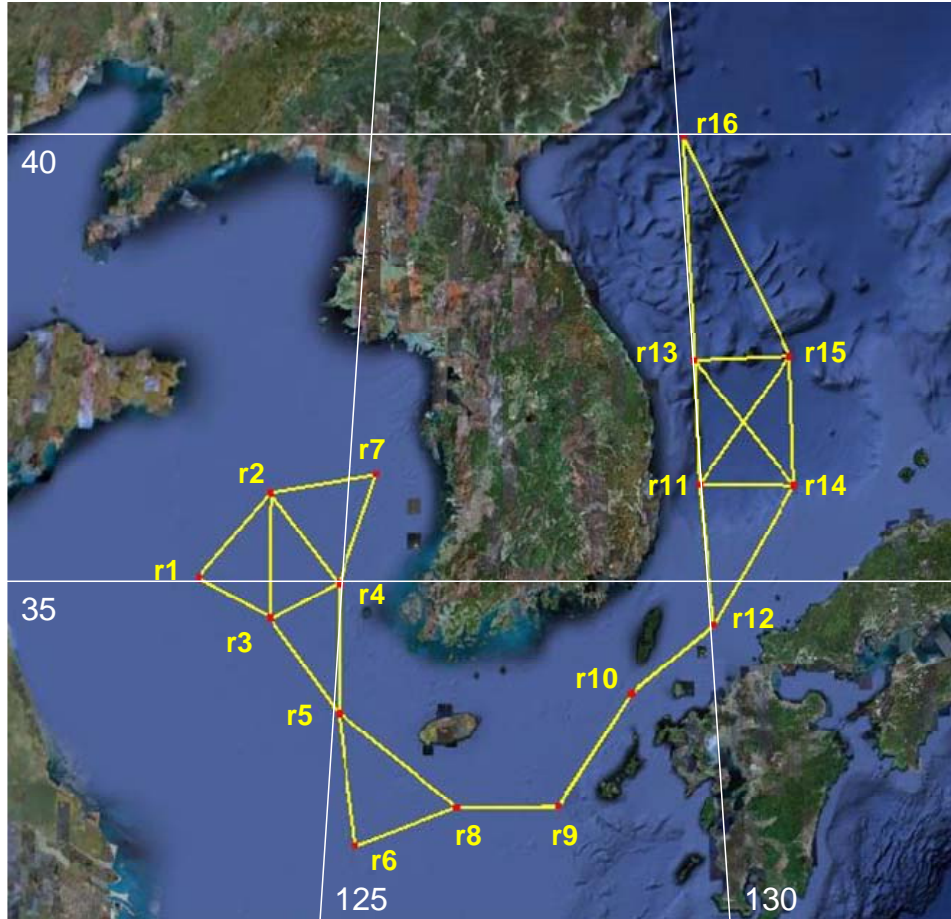
The collection of available information concerning foreign nations, hostile or potentially hostile forces or elements, or areas of actual or potential operations. (JP 1-02, 2001)

*k. Submarine Intelligence Collection (SubIntel)*

The previous ten mission types are also used in Dugan (2007). We have added SubIntel, a user-defined mission, to illustrate the flexibility of this planning tool through its ability to adapt to *any* list of mission types. We define SubIntel as an intelligence collection mission that can only be performed by a submarine.

## **2. Theater of Operations**

The unclassified scenario considers a notional series of events on the Korean peninsula leading to U.S. and South Korean Combined Forces Command action in the region. U.S. Pacific Command orders naval assets to the region, beginning with forward deployed forces and surging additional assets from outside the theater. Figure 4 shows the area of operations surrounding the Korean Peninsula divided into 16 regions. The vertical gridlines depict degrees of east longitude, and the horizontal gridlines depict degrees of north latitude. Appendix A contains the NMP Region worksheet in which we define the regions and arcs for our scenario.



**Figure 4. Scenario Region.** The notional scenario takes place in the waters surrounding the Korean Peninsula. The horizontal gridlines represent degrees of north latitude. Vertical gridlines represent degrees of east longitude. Each gridline is approximate, and longitudinal lines appear to slope due to the simple cylindrical projection of the map. 16 regions, or waypoints, depict the area of operations. Regions and the arcs connecting them are user-defined inputs to Navy Mission Planner (Adapted From: Google Earth, 2009).

### 3. Resources

The surge ships arrive in theater sequentially. Due to the rapidly escalating situation, not all forces are on station when hostilities commence. Table 1 depicts the ship input to NMP used in this scenario as well as an additional, unused ship, which demonstrates the use of the Available column. Appendix B shows the entire ship set, including all ships not used in the scenario.

From this, one can discern the flow into theater. Notionally, two cruisers, four destroyers, and two fast-attack submarines are forward deployed and available on day one of the fifteen-day planning horizon. On day four, a surface action group consisting of a cruiser, three destroyers, and two frigates arrive on station. On day six, the third fast-attack submarine arrives at region r7. Finally, on day seven, the last units arrive. These are a cruiser, destroyer, and frigate.

**Table 1. NMP Ship Resources.** The user inputs available ships by hull number, name, availability, ship class, type, start day, start region, and available CMCs. For example, USS Kidd, DDG 100 is available for tasking on day four and begins in region r5. CMCs C13, C16, and C19 are available to Kidd. Note also that CG 63, USS Cowpens, is not available for this scenario.

| Ship   | Name            | Avail | Class | Type   | Start Day | Start Region | CMCs |     |     |
|--------|-----------------|-------|-------|--------|-----------|--------------|------|-----|-----|
| CG61   | Monterey        | x     | CG    | COMBAT | 1         | r2           | C1   | C5  | C7  |
| CG66   | Hue City        | x     | CG    | COMBAT | 1         | r13          | C2   | C5  | C8  |
| CG72   | Vella Gulf      | x     | CG    | COMBAT | 4         | r7           | C3   | C6  | C9  |
| CG58   | Philippine Sea  | x     | CG    | COMBAT | 7         | r10          | C4   | C5  | C10 |
| CG63   | Cowpens         |       | CG    | COMBAT |           |              |      |     |     |
| DDG53  | John Paul Jones | x     | DDG   | COMBAT | 1         | r1           | C11  | C15 | C17 |
| DDG54  | Curtis Wilbur   | x     | DDG   | COMBAT | 1         | r4           | C11  | C15 | C17 |
| DDG86  | Shoup           | x     | DDG   | COMBAT | 1         | r9           | C12  | C15 | C18 |
| DDG90  | Chaffee         | x     | DDG   | COMBAT | 1         | r7           | C12  | C15 | C18 |
| DDG100 | Kidd            | x     | DDG   | COMBAT | 4         | r5           | C13  | C16 | C19 |
| DDG80  | Roosevelt       | x     | DDG   | COMBAT | 4         | r13          | C11  | C15 | C17 |
| DDG104 | Sterett         | x     | DDG   | COMBAT | 4         | r4           | C11  | C15 | C17 |
| DDG97  | Halsey          | x     | DDG   | COMBAT | 7         | r11          | C11  | C15 | C17 |
| FFG48  | Vandegrift      | x     | FFG   | COMBAT | 4         | r10          | C21  | C25 |     |
| FFG52  | Carr            | x     | FFG   | COMBAT | 4         | r11          | C22  | C25 |     |
| FFG47  | Nicholas        | x     | FFG   | COMBAT | 7         | r8           | C23  | C26 |     |
| SSN752 | Pasadena        | x     | SSN   | COMBAT | 1         | r12          | C31  | C37 |     |
| SSN718 | Honolulu        | x     | SSN   | COMBAT | 6         | r7           | C34  | C37 |     |
| SSN717 | Olympia         | x     | SSN   | COMBAT | 1         | r16          | C33  | C37 |     |

Table 2 shows an example CMC list for the cruiser ship class. Appendix C shows the entire CMC matrix for our scenario. C1 is the full concurrent mission capability for a cruiser's core missions of AD, ASW, SUW, Strike, and NSFS. C2, C3, and C4 depict examples of degradations from C1 in which full capability is unavailable for some missions. C5 and C6 are options for MIO. One may interpret C5 as the base case in which the staff planner chooses not to assign a cruiser with TBMD, ASW, or NSFS when that cruiser is assigned a MIO mission. C6 is similar to C5, but it provides a degraded

capability in SUW. C7, C8, C9 and C10 are options for TBMD in which AD is zero. C8 through C10 are examples of degraded concurrent capabilities for TBMD. The operational planner is free to modify the CMC matrix to fit any necessary combination of capabilities and casualties. The standard, full mission capable CMCs for a cruiser are C1, C5, and C7. The majority of ships listed in Table 1 are operating with degraded mission capabilities.

**Table 2. CMC Matrix for CG Class of Ships.** CMC matrix is a user-defined input. The operational planner keeps track of ships' system status and adjusts the matrix accordingly. For example, C1 shows that a cruiser can complete AD, ASW, SUW, Strike, NSFS, and Intel concurrently and to 100% completion. C2 shows a situation in which a ship has casualties or shortfalls affecting its ability to perform ASW and NSFS, which can only be accomplished at 50% and 75% of normal effectiveness, respectively. Note that the planner should not assign C1 if a ship has mission degradations C2, C3, or C4.

|            |     | Mission |      |     |     |        |      |     |     |      |       |          |
|------------|-----|---------|------|-----|-----|--------|------|-----|-----|------|-------|----------|
| Ship Class | CMC | AD      | TBMD | ASW | SUW | Strike | NSFS | MIO | MCM | Mine | Intel | SubIntel |
| CG         | C1  | 1       | 0    | 1   | 1   | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C2  | 1       | 0    | 0.5 | 1   | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C3  | 1       | 0    | 1   | 0.5 | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C4  | 1       | 0    | 0   | 1   | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C5  | 1       | 0    | 0   | 1   | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C6  | 1       | 0    | 0   | 0.5 | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C7  | 0       | 1    | 1   | 1   | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C8  | 0       | 1    | 0.5 | 1   | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C9  | 0       | 1    | 1   | 0.5 | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C10 | 0       | 1    | 0   | 1   | 1      | 1    | 0   | 0   | 0    | 1     | 0        |

#### 4. Priorities and Requirements

Day one represents the start of the deterrence phase of joint operations, Phase I (JP 3-0, 2006), during which naval units perform AD, TBMD, ASW, MIO, and intelligence collection. In Phase I the ships patrol regions prioritized in four groups. TBMD in region r2, ASW in r12, and SubIntel in r16 are highest priorities. Regions r1, r7, and r13 are next priority as these are the extreme western and northern regions. Regions r4, r9, and r11 are third priority because r4 and r11 are the second most northern regions and r9 closes the ring around the peninsula. The remaining regions are lowest priority.

Mission values reflect these priorities. Region r2 is the designated TBMD sector. Region r12 is a chokepoint facilitating north/south and east/west flow. Enemy submarines are the chief threat in this region, and ASW is the top priority here. Region r16, in international waters, provides a northern vantage point for intelligence collection. To ensure these missions are fully covered, we assign value 20. We assign values to MIO, AD, ASW, and Intel according to regional priorities. The missions in the second priority regions have values 9, 7, 8, and 7 respectively. The values reduce by two for each lower priority.

On day five, Phase II operations to seize the initiative begin (JP 3-0, 2006). Phase II is the de facto commencement of offensive operations. Required missions include SUW, Strike, and NSFS in addition to those begun on day one. Phase II runs through the end of the scenario, day fifteen. TBMD in region r2, ASW in region r12, and SubIntel in region r16 remain the top priority as in Phase I. Regions r5, r7, and r13 are next priority, followed by regions r4, r10, and r11, then regions r8 and r9. The reasoning for the prioritization of regions follows similar logic to the process of Phase I. Strike missions in regions r5, r7, and r13 are the highest remaining priority and take a value of 15. Values for NSFS, SUW, MIO, and ASW begin at 9, 7, 7, 5, and 5 respectively. Values again reduce by two for each succeeding priority level. Appendix D contains the entire mission set for our scenario. Table 3 shows a portion of this set for the first five scenario regions.

**Table 3. NMP Missions Input.** Required mission type, region, time horizon, value, and prerequisite missions are input via the Mission worksheet of NMP. This table shows missions for the first five regions. For example, TBMD in region r2 appears for all 15 scenario days and has a value of 20. AD is a prerequisite mission for TBMD, but is not explicitly scheduled for the initial run.

| Mission | Include | Type   | Region | Start Day | End Day | Value | Requires |     |
|---------|---------|--------|--------|-----------|---------|-------|----------|-----|
| m1      | x       | MIO    | r1     | 1         | 4       | 9     | AD       |     |
| m2      | x       | AD     | r1     | 1         | 4       | 7     |          |     |
| m3      | x       | ASW    | r1     | 1         | 4       | 8     | AD       | SUW |
| m4      | x       | Intel  | r1     | 1         | 4       | 7     |          |     |
| m5      | x       | TBMD   | r2     | 1         | 15      | 20    | AD       |     |
| m6      | x       | MIO    | r3     | 1         | 4       | 5     | AD       |     |
| m7      | x       | AD     | r3     | 1         | 15      | 3     |          |     |
| m8      | x       | ASW    | r3     | 1         | 4       | 4     | AD       |     |
| m9      | x       | Intel  | r3     | 1         | 15      | 3     |          |     |
| m10     | x       | MIO    | r4     | 1         | 4       | 7     | AD       |     |
| m11     | x       | AD     | r4     | 1         | 15      | 5     |          |     |
| m12     | x       | ASW    | r4     | 1         | 4       | 6     | SUW      |     |
| m13     | x       | Intel  | r4     | 1         | 15      | 5     |          |     |
| m14     | x       | Strike | r4     | 5         | 11      | 7     | AD       |     |
| m15     | x       | NSFS   | r4     | 5         | 8       | 5     | AD       |     |
| m16     | x       | SUW    | r4     | 5         | 11      | 5     | AD       |     |
| m17     | x       | MIO    | r4     | 12        | 15      | 3     | AD       |     |
| m18     | x       | ASW    | r4     | 12        | 15      | 3     | SUW      |     |
| m19     | x       | MIO    | r5     | 1         | 4       | 5     | AD       |     |
| m20     | x       | AD     | r5     | 1         | 15      | 3     |          |     |
| m21     | x       | ASW    | r5     | 1         | 4       | 4     | SUW      |     |
| m22     | x       | Intel  | r5     | 1         | 15      | 3     |          |     |
| m23     | x       | Strike | r5     | 5         | 11      | 15    | AD       |     |
| m24     | x       | NSFS   | r5     | 5         | 8       | 7     | AD       |     |
| m25     | x       | SUW    | r5     | 5         | 11      | 7     | AD       |     |
| m26     | x       | MIO    | r5     | 12        | 15      | 5     | AD       |     |
| m27     | x       | ASW    | r5     | 12        | 15      | 5     | SUW      |     |

## B. RESULTS

This research investigates four runs of the scenario. We explore methods the operational planner may use to improve the results NMP provides. Each run uses a maximum of 750,000 total schedules and 75,000 maximum schedules per ship.

### 1. Initial Run

We first run the model using a value for max stall days of three days. We achieve a total mission value of 2416.50, with an upper bound of 2535.50. Scanning the output, we check for completions of missions with prerequisites. If any prerequisite mission is not accomplished, then there is a gap in accomplishment of the main mission as well. For



example, Appendix D lists missions m3, m12, and m21 as ASW missions with an SUW prerequisite mission. As the operators in this scenario, we do not assign a SUW mission for the first four scenario days. As a result, these ASW missions are gapped, except on day four in region r5. On this day, DDG 100 and DDG 54 perform SUW, allowing completion of mission m21, ASW. This result is shown in Table 4. Note that the SUW mission accrues no value, because it is not a user-assigned mission for that region or day.

Knowing that the maritime commander is most interested in the highest priority missions, we track the completion of these. We see that the high-priority TBMD mission takes place only on day fifteen. While TBMD in region r2 has a value of 20 and is one of the three highest priority missions, there is not enough air defense support. AD is a prerequisite mission, but it is not explicitly assigned in the Missions worksheet; therefore, it would accrue no value. NMP can find more value in other, lower-valued missions rather than assigning transit days to move a second asset to region r2 and perform zero-value AD.

The second high-priority mission, ASW in region r12, is gapped on days four through six. On seven of the nine succeeding days, it only accrues half-value. With limited resources, a ship degraded in ASW must perform the mission.

NMP gaps the SubIntel mission on ten of the fifteen days in the scenario. SSN 717 begins the scenario in r16 and performs the SubIntel mission for the first three days. Once the max stall days limit is reached, it moves on. Due to the long transit distance, NMP assigns no other sub until day nine, for one day only, then again until day fifteen.

**Table 4. Selected Mission Accomplishments.** This table displays selected mission accomplishment output. The column Value is the user-assigned value for the mission. Effort is the decision variable U, the level of accomplishment for that mission in that region on that day. The column Achieved is the portion of the objective value achieved by accomplishing the given mission in the given region on the given day and is the product of Value and Effort. For example, on day four in region five, mission SUW has no value, but is performed fully, that is to a level of one. The column Achieve is zero, and there is no contribution to objective value. This prerequisite mission allows completion of ASW on day four in region five, with a value of four, effort of one, and achieved value of four.

| MISSION ACCOMPLISHMENT |          |     |       |        |          |
|------------------------|----------|-----|-------|--------|----------|
| Region                 | Mission  | Day | Value | Effort | Achieved |
| r1                     | ASW      | d4  | 8     | 0      | 0        |
| r4                     | ASW      | d4  | 6     | 0      | 0        |
| r5                     | SUW      | d4  | 0     | 1      | 0        |
| r5                     | ASW      | d4  | 4     | 1      | 4        |
|                        |          |     |       |        |          |
| r2                     | AD       | d1  | 0     | 1      | 0        |
| r2                     | AD       | d15 | 0     | 1      | 0        |
| r2                     | TBMD     | d15 | 20    | 1      | 20       |
|                        |          |     |       |        |          |
| r12                    | ASW      | d4  | 20    | 0      | 0        |
| r12                    | ASW      | d5  | 20    | 0      | 0        |
| r12                    | ASW      | d6  | 20    | 0      | 0        |
|                        |          |     |       |        |          |
| r16                    | SubIntel | d1  | 20    | 0      | 0        |
| r16                    | SubIntel | d2  | 20    | 0      | 0        |
| r16                    | SubIntel | d3  | 20    | 0      | 0        |
| r16                    | SubIntel | d9  | 20    | 0      | 0        |
| r16                    | SubIntel | d15 | 20    | 0      | 0        |

## 2. Second Run—Assign AD in Region r2

The operational commander's first reaction to hearing that TBMD, one of the number-one priority missions, is gapped for fourteen days would be to order assets moved to that region to do the mission. For the second run, two changes are made to the scenario. First, as shown in Table 5, the user schedules AD in region r2 for the duration of the planning horizon. Note that the value is 20, commensurate with the value of the TBMD mission.

**Table 5. Example of Ensuring High Priority Prerequisite Missions.** AD is a prerequisite mission for TBMD in region r2 for each day in the planning horizon. In the original scenario, the operational planner does not schedule the AD mission. The planner lets NMP decide if there is more value in assigning an AD asset to the high-priority TBMD mission, or to assigning the two assets elsewhere. By adding a dedicated requirement for AD in region r2 and valuing it according to the value of TBMD, in this case 20, the planner attempts to ensure that NMP schedules the commander’s highest priority mission.

| Mission | Include | Type | Region | Start Day | End Day | Value | Requires |
|---------|---------|------|--------|-----------|---------|-------|----------|
| m80     | x       | AD   | r2     | 1         | 15      | 20    |          |

The second change is illustrated in Table 6, which shows the assignment of DDG 54 to region r2 on day one of the planning horizon. This change assigns a second asset to the region in order to meet mission requirements.

**Table 6. Example of Assigning a Ship to the Region Corresponding to a High Priority Prerequisite Mission.** In the original scenario, DDG 54 begins in region r4. For the second and succeeding runs, DDG 54 begins in region r2. There are now two assets assigned to begin operations in region r2, corresponding to two mission requirements.

| Ship  | Name          | Avail | Class | Type   | Start Day | Start Region | CMCs        |
|-------|---------------|-------|-------|--------|-----------|--------------|-------------|
| DDG54 | Curtis Wilbur | x     | DDG   | COMBAT | 1         | r2           | C11 C15 C17 |

The results of these changes are mixed. Objective value improves to 2737.00, with an upper bound of 2749.67. The prerequisite for TBMD, AD, is scheduled for the entire planning horizon. TBMD appears for the first three days, but the enumeration limit on max stall days forces the ships to move from region r2. DDG 53 moves into the region to perform AD, but a second asset is not available to perform TBMD. TBMD is gapped from day four until it resumes for days 14 and 15.

The ASW mission in region r12 and the SubIntel mission in region r16 are unchanged. The ASW gap remains on days four, five, and six, and SubIntel again takes place only on days one through three, nine, and fifteen.

### 3. Third Run—Extend *Max Stall Days* to Seven

The second run gives us an improvement over the first in that NMP fully schedules AD in region r2. There is an assignment shortfall, however, because the max

stall days constraint forces ships out of not only the highest priority regions where the highest priority missions occur, but out of all regions after three days. The third run extends max stall days to seven in an attempt to improve mission completion values.

In the third run, objective value again improves to 2940.00, with an upper bound of 2961.00. AD in region r2 occurs each day of the planning horizon. The TBMD assignment is improved compared to the second run. TBMD occurs for the first seven days, and then it is gapped for the next four. TBMD is again scheduled in region r2 for days twelve through fifteen. Again NMP allows CG 61 and DDG 54 to maintain station until the expiration of the max stall days, at which time there is a four day gap until two assets are available in region r2.

DDG 53 moves into region r2 on day five, after completing the AD, MIO, and Intel requirements in region r1 for the first four days. NMP determines that this is the ship to take over AD in region r2 on day eight. DDG 53 has no better mission within transit range of region r1 for days five through seven, so it moves into region r2 early, meaning three assets are in that region covering the two missions. Table 7 illustrates the mission accomplishment for TBMD and AD in region r2.

**Table 7. Air Defense and TBMD Mission Accomplishments in Region r2.** AD and TBMD take place in region r2 for the first seven days of the scenario. Once the constraint max stall days is reached, the assigned ships move on to other regions. We see that while AD is covered every day, TBMD has a four day gap beginning on day eight.

| MISSION ACCOMPLISHMENT |         |     |       |        |          |
|------------------------|---------|-----|-------|--------|----------|
| Region                 | Mission | Day | Value | Effort | Achieved |
| r2                     | AD      | d1  | 20    | 1      | 20       |
| r2                     | AD      | d2  | 20    | 1      | 20       |
| r2                     | AD      | d3  | 20    | 1      | 20       |
| r2                     | AD      | d4  | 20    | 1      | 20       |
| r2                     | AD      | d5  | 20    | 1      | 20       |
| r2                     | AD      | d6  | 20    | 1      | 20       |
| r2                     | AD      | d7  | 20    | 1      | 20       |
| r2                     | AD      | d8  | 20    | 1      | 20       |
| r2                     | AD      | d9  | 20    | 1      | 20       |
| r2                     | AD      | d10 | 20    | 1      | 20       |
| r2                     | AD      | d11 | 20    | 1      | 20       |
| r2                     | AD      | d12 | 20    | 1      | 20       |
| r2                     | AD      | d13 | 20    | 1      | 20       |
| r2                     | AD      | d14 | 20    | 1      | 20       |
| r2                     | AD      | d15 | 20    | 1      | 20       |
|                        |         |     |       |        |          |
| r2                     | TBMD    | d1  | 20    | 1      | 20       |
| r2                     | TBMD    | d2  | 20    | 1      | 20       |
| r2                     | TBMD    | d3  | 20    | 1      | 20       |
| r2                     | TBMD    | d4  | 20    | 1      | 20       |
| r2                     | TBMD    | d5  | 20    | 1      | 20       |
| r2                     | TBMD    | d6  | 20    | 1      | 20       |
| r2                     | TBMD    | d7  | 20    | 1      | 20       |
| r2                     | TBMD    | d12 | 20    | 1      | 20       |
| r2                     | TBMD    | d13 | 20    | 1      | 20       |
| r2                     | TBMD    | d14 | 20    | 1      | 20       |
| r2                     | TBMD    | d15 | 20    | 1      | 20       |

ASW in region r12 is scheduled for all fifteen days of the planning horizon. On two particular days, nine and ten, ASW is accomplished to the 0.5 level. FFG 52 performs ASW on these days, but is a degraded ASW platform.

SubIntel in region r16 is gapped after the seventh day. There is a two-day gap until another submarine completes the transit and takes over the mission on day ten.

#### **4. Fourth Run—Allow Unlimited Stall Days**

The fourth run yields the highest objective value of 3503.50, with an upper bound of 3507.50. This final run of our scenario shows full completion of each of the three highest priority missions. From an enumeration standpoint, the schedules are less diverse. As ships are allowed to delay longer in one region, more schedules have the same regions repeating. It is important to enumerate enough varied schedules to have confidence in finding the optimal set of employment schedules, as opposed to finding the best one of a limited set. Table 8 captures a selected portion of the mission completions for the missions of interest, and Table 9 shows the employment schedules for the ships involved in the region r2 TBMD mission and the region r16 SubIntel mission.

**Table 8. Mission Accomplishments for Selected High Priority Missions.** In the fourth scenario run, all three high priority missions are fully accomplished on each day of the planning horizon. This table presents selected results. For region r2 missions, a scan of Appendix F shows that CG 61 and DDG 54 begin the scenario in region r2 performing AD and TBMD. CG 61 remains through day thirteen, and DDG 54 remains through day fourteen. On day five, DDG 53 moves into the region and stays through day fourteen. CG 72 and DDG 90 move into the region to close out the scenario on day fifteen.

| MISSION ACCOMPLISHMENT |          |     |       |        |          |
|------------------------|----------|-----|-------|--------|----------|
| Region                 | Mission  | Day | Value | Effort | Achieved |
| r2                     | TBMD     | d1  | 20    | 1      | 20       |
| r2                     | TBMD     | d2  | 20    | 1      | 20       |
| r2                     | TBMD     | d3  | 20    | 1      | 20       |
| r2                     | TBMD     | d4  | 20    | 1      | 20       |
|                        |          | ... |       |        |          |
| r2                     | TBMD     | d12 | 20    | 1      | 20       |
| r2                     | TBMD     | d13 | 20    | 1      | 20       |
| r2                     | TBMD     | d14 | 20    | 1      | 20       |
| r2                     | TBMD     | d15 | 20    | 1      | 20       |
|                        |          |     |       |        |          |
| r12                    | ASW      | d1  | 20    | 1      | 20       |
| r12                    | ASW      | d2  | 20    | 1      | 20       |
| r12                    | ASW      | d3  | 20    | 1      | 20       |
| r12                    | ASW      | d4  | 20    | 1      | 20       |
|                        |          | ... |       |        |          |
| r12                    | ASW      | d12 | 20    | 1      | 20       |
| r12                    | ASW      | d13 | 20    | 1      | 20       |
| r12                    | ASW      | d14 | 20    | 1      | 20       |
| r12                    | ASW      | d15 | 20    | 1      | 20       |
|                        |          |     |       |        |          |
| r16                    | SubIntel | d1  | 20    | 1      | 20       |
| r16                    | SubIntel | d2  | 20    | 1      | 20       |
| r16                    | SubIntel | d3  | 20    | 1      | 20       |
| r16                    | SubIntel | d4  | 20    | 1      | 20       |
|                        |          | ... |       |        |          |
| r16                    | SubIntel | d12 | 20    | 1      | 20       |
| r16                    | SubIntel | d13 | 20    | 1      | 20       |
| r16                    | SubIntel | d14 | 20    | 1      | 20       |
| r16                    | SubIntel | d15 | 20    | 1      | 20       |

**Table 9. Employment Schedule for SSN 717.** SSN 717 is assigned to region r16 on day one of the scenario. With *max stall days* unlimited and the long distance to adjacent regions, this submarine is allowed to remain in region r16 and complete the high-priority SubIntel mission.

| COMBAT SHIP EMPLOYMENT SCHEDULE |         |          |  |  |
|---------------------------------|---------|----------|--|--|
| SSN717                          | p708340 |          |  |  |
| d1                              | r16     | SubIntel |  |  |
| d2                              | r16     | SubIntel |  |  |
| d3                              | r16     | SubIntel |  |  |
| d4                              | r16     | SubIntel |  |  |
| d5                              | r16     | SubIntel |  |  |
| d6                              | r16     | SubIntel |  |  |
| d7                              | r16     | SubIntel |  |  |
| d8                              | r16     | SubIntel |  |  |
| d9                              | r16     | SubIntel |  |  |
| d10                             | r16     | SubIntel |  |  |
| d11                             | r16     | SubIntel |  |  |
| d12                             | r16     | SubIntel |  |  |
| d13                             | r16     | SubIntel |  |  |
| d14                             | r16     | SubIntel |  |  |
| d15                             | r16     | SubIntel |  |  |

### C. LESSONS LEARNED

We have found that initial positioning of ships on their first day in theater can have a significant effect on the total mission value obtained by NMP. The operational planner knows the commander's highest priority missions and regions. The planner is also aware of what ships are under his or her commander's operational control and for what time period. We have found that when a high priority mission has a prerequisite mission, e.g., AD is a prerequisite for TBMD, the planner should schedule the prerequisite mission and value it accordingly.

We have noted that increasing stall days can keep ships in place to accomplish important missions in a region. With limited resources or large distances between regions, the max stall days constraint may force ships to leave priority regions. As a result, high-priority missions may be left uncovered while ships are in transit. Planners can solve this issue by increasing the max stall days.

As the constraint max stall days increases, there are more schedules with the same regions repeated. In response, the planner should increase the constraint max schedules



and max schedules per ship to allow NMP to enumerate more varied schedules. More varied schedules increases the likelihood of finding the true optimal schedule. The number is “high enough” when increasing it fails to improve the value of the objective equation.

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## **V. SUMMARY AND FUTURE IMPROVEMENTS**

### **A. SUMMARY**

Maritime component commanders employ forces in support of the combatant commander. When requirements exceed resources, planners must assign available resources efficiently to maximize mission completions. NMP seeks to reduce the time involved in mission planning by taking the planner's inputs and returning a set of optimized ship employment schedules.

NMP uses Microsoft Excel and Visual Basic code to enumerate a set of feasible candidate schedules for each ship subject to the user-defined maximum number of schedules as well as the maximum number of schedules per ship. Excel sends the set of inputs to GAMS which uses a commercial solver to find the optimal set of mission schedules that maximizes the value of assigned missions.

### **B. FUTURE IMPROVEMENTS**

#### **1. Common Operating Picture**

Dugan (2007) recommends that NMP interact with the Common Operating Picture. This functionality is not yet realized; however, it should remain a goal that NMP receive automatic updates to ship position and readiness levels, so as to provide daily updates as an operational plan unfolds in real time.

#### **2. Logistics**

Replenishment of stores is not addressed in NMP. Every few days a ship must take on fuel, food, weapons, parts, and sometimes transfer personnel. In the current scenario, ships remain available for tasking or transit for the entire planning horizon. Future versions of NMP should explicitly model logistics requirements, possibly through the inclusion of Combat Logistics Force ships, and track re-supply schedules and weapons load outs.

The majority of the ships in this scenario have degradations. The addition of logistics to this model would add to the realism of the solution and allow degraded units to become full mission capable over the course of the scenario.

### **3. User Interface**

Further refinement of the NMP user interface is possible. The raw output is a lengthy text file and a few Excel worksheets. Refinement of the output reports which highlight the gaps in mission coverage would be helpful to the operational planner. Automatic output of Gantt charts showing ship employment schedules would save the user much preparation time for briefing the commander.

### **4. Improve Enumeration for More Diverse Schedules**

As the planning horizon and number of regions grow, the total number of possible schedules grows exponentially. The current version of NMP breaks down at about one million total schedules due to system memory requirements. Instead of increasing the total number of schedules used in the optimization model, it would be more productive to produce a more diverse subset of feasible schedules. This would be accomplished by a modification of the enumeration algorithm itself, or by using another model or algorithm to filter millions of schedules down to a few thousand (per ship) that are likely to be useful.

### **5. Platform Pre-positioning**

Initial positioning of ships for the first scenario day has a major impact on the solutions achieved by NMP. The next version of NMP can be expanded to allow flexibility in the first day's schedules. A minor modification to the interface, which does not change the underlying model, would incorporate a new column, "Pre-positioned," into the Ships worksheet. If this column is checked for a particular ship, then all schedules for that ship would begin in the region specified by the user. Otherwise, a greedy start-point generator would position the ships in regions with high-valued missions. This modification would allow the operational commander more flexibility for the initial day of the planning horizon.

## APPENDIX A. REGION AND ARC DEFINITIONS

The following table displays the NMP region set for the scenario presented in Chapter IV. We present 16 regions and 25 arcs. For example, region r16 is defined at 40 degrees north latitude and 130 degrees east longitude. Region r16 is connected to r13 at a distance of 150 nautical miles and to r15 at a distance of 165.7 nautical miles.

| Region | LON    | LAT   |  | Arcs |     | Length(nm) |
|--------|--------|-------|--|------|-----|------------|
| r1     | 123    | 35    |  | r1   | r2  | 77.4       |
| r2     | 124    | 36    |  | r1   | r3  | 57.7       |
| r3     | 124    | 34.5  |  | r2   | r3  | 90         |
| r4     | 125    | 35    |  | r2   | r4  | 77.4       |
| r5     | 125    | 33.56 |  | r2   | r7  | 74.3       |
| r6     | 125.25 | 32    |  | r3   | r4  | 57.7       |
| r7     | 125.5  | 36.25 |  | r3   | r5  | 75.2       |
| r8     | 126.6  | 32.5  |  | r4   | r7  | 78.9       |
| r9     | 128    | 32.5  |  | r4   | r5  | 86.4       |
| r10    | 129    | 33.8  |  | r5   | r6  | 94.5       |
| r11    | 130    | 36    |  | r5   | r8  | 102.6      |
| r12    | 130.2  | 34.5  |  | r6   | r8  | 74.8       |
| r13    | 130    | 37.5  |  | r8   | r9  | 70.9       |
| r14    | 131.5  | 36    |  | r9   | r10 | 92.8       |
| r15    | 131.5  | 37.5  |  | r10  | r12 | 72.9       |
| r16    | 130    | 40    |  | r11  | r12 | 90.6       |
|        |        |       |  | r11  | r13 | 90         |
|        |        |       |  | r11  | r14 | 72.8       |
|        |        |       |  | r11  | r15 | 115.4      |
|        |        |       |  | r12  | r14 | 110.3      |
|        |        |       |  | r13  | r14 | 115.4      |
|        |        |       |  | r13  | r15 | 71.4       |
|        |        |       |  | r14  | r15 | 90         |
|        |        |       |  | r13  | r16 | 150        |
|        |        |       |  | r15  | r16 | 165.7      |

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## APPENDIX B. FULL SHIP SET

The following table displays the full NMP ship worksheet for the scenario presented in Chapter IV. Inputs include hull number, ship name, availability flag, ship class, ship type, start day, start region, and the available CMC set for that ship. For example, USS Curtis Wilbur, DDG 54, is available in the scenario. It is a guided missile destroyer, DDG, classified as a combat ship. Curtis Wilbur begins on day one in region r4 and has CMC set C11, C15, and C17 (see Appendix C for the full listing of CMC sets in our scenario). Note that all ship types are listed as combat ships. This column enables future development to include logistics forces.

| Ship   | Name            | Avail | Class | Type   | Start Day | Start Region | CMCs |     |     |
|--------|-----------------|-------|-------|--------|-----------|--------------|------|-----|-----|
| CG61   | Monterey        | x     | CG    | COMBAT | 1         | r2           | C1   | C5  | C7  |
| CG66   | Hue City        | x     | CG    | COMBAT | 1         | r13          | C2   | C5  | C8  |
| CG72   | Vella Gulf      | x     | CG    | COMBAT | 4         | r7           | C3   | C6  | C9  |
| CG58   | Philippine Sea  | x     | CG    | COMBAT | 7         | r10          | C4   | C5  | C10 |
| CG63   | Cowpens         |       | CG    | COMBAT | 50        | r20          | C1   |     |     |
| CG56   | San Jacinto     |       | CG    | COMBAT | 50        | r20          | C1   |     |     |
| CG65   | Chosin          |       | CG    | COMBAT | 50        | r20          | C1   |     |     |
| DDG53  | John Paul Jones | x     | DDG   | COMBAT | 1         | r1           | C11  | C15 | C17 |
| DDG54  | Curtis Wilbur   | x     | DDG   | COMBAT | 1         | r4           | C11  | C15 | C17 |
| DDG86  | Shoup           | x     | DDG   | COMBAT | 1         | r9           | C12  | C15 | C18 |
| DDG90  | Chaffee         | x     | DDG   | COMBAT | 1         | r7           | C12  | C15 | C18 |
| DDG100 | Kidd            | x     | DDG   | COMBAT | 4         | r5           | C13  | C16 | C19 |
| DDG80  | Roosevelt       | x     | DDG   | COMBAT | 4         | r13          | C11  | C15 | C17 |
| DDG104 | Sterett         | x     | DDG   | COMBAT | 4         | r4           | C11  | C15 | C17 |
| DDG97  | Halsey          | x     | DDG   | COMBAT | 7         | r11          | C11  | C15 | C17 |
| DDG78  | Porter          |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG74  | McFaul          |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG72  | Mahan           |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG75  | Donald Cook     |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG71  | Ross            |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG62  | Fitzgerald      |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |
| DDG67  | Cole            |       | DDG   | COMBAT | 50        | r20          | C11  |     |     |

| Ship    | Name           | Avail | Class | Type   | Start Day | Start Region | CMCs |     |  |
|---------|----------------|-------|-------|--------|-----------|--------------|------|-----|--|
| FFG48   | Vandegrift     | x     | FFG   | COMBAT | 4         | r10          | C21  | C25 |  |
| FFG52   | Carr           | x     | FFG   | COMBAT | 4         | r11          | C22  | C25 |  |
| FFG47   | Nicholas       | x     | FFG   | COMBAT | 7         | r8           | C23  | C26 |  |
| FFG60   | Rodney M Davis |       | FFG   | COMBAT | 50        | r20          | C21  |     |  |
| LCS1    | Freedom        |       | LCS   | COMBAT | 50        | r20          | C27  |     |  |
| LCS2    | Independence   |       | LCS   | COMBAT | 50        | r20          | C27  |     |  |
| SSN752  | Pasadena       | x     | SSN   | COMBAT | 1         | r12          | C31  | C37 |  |
| SSN718  | Honolulu       | x     | SSN   | COMBAT | 6         | r7           | C34  | C37 |  |
| SSN717  | Olympia        | x     | SSN   | COMBAT | 1         | r16          | C33  | C37 |  |
| SSN770  | Tucson         |       | SSN   | COMBAT | 50        | r20          | C31  |     |  |
| SSN706  | Albuquerque    |       | SSN   | COMBAT | 50        | r20          | C31  |     |  |
| SSN764  | Boise          |       | SSN   | COMBAT | 50        | r20          | C31  |     |  |
| SSGN726 | Ohio           |       | SSGN  | COMBAT | 50        | r20          | C38  |     |  |
| MCM6    | Devastator     |       | MCM   | COMBAT | 50        | r20          | C41  |     |  |
| MCM8    | Scout          |       | MCM   | COMBAT | 50        | r20          | C41  |     |  |
| MCM10   | Warrior        |       | MCM   | COMBAT | 50        | r20          | C41  |     |  |
| MCM14   | Chief          |       | MCM   | COMBAT | 50        | r20          | C41  |     |  |



## APPENDIX C. FULL CMC MATRIX

The following table displays the NMP concurrent mission capability matrix for the scenario presented in Chapter IV. Rows with values less than one represent mission capability degradations. LCS, SSGN, and MCM class ships are available but not used in the scenario. We define available CMCs to enable easy expansion of the scenario. For example, CMC C12 belongs to the DDG class and represents full concurrent mission capability in air defense, surface warfare, strike, and intelligence collection, but degradations to half-capability in antisubmarine warfare and three-quarter capability in naval surface fire support.

| Ship Class | CMC | Mission |      |      |      |        |      |     |     |      |       |          |
|------------|-----|---------|------|------|------|--------|------|-----|-----|------|-------|----------|
|            |     | AD      | TBMD | ASW  | SUW  | Strike | NSFS | MIO | MCM | Mine | Intel | SubIntel |
| CG         | C1  | 1       | 0    | 1    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C2  | 1       | 0    | 0.5  | 1    | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C3  | 1       | 0    | 1    | 0.5  | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C4  | 1       | 0    | 0    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C5  | 1       | 0    | 0    | 1    | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C6  | 1       | 0    | 0    | 0.5  | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C7  | 0       | 1    | 1    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C8  | 0       | 1    | 0.5  | 1    | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C9  | 0       | 1    | 1    | 0.5  | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C10 | 0       | 1    | 0    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
| DDG        | C11 | 1       | 0    | 1    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C12 | 1       | 0    | 0.5  | 1    | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C13 | 1       | 0    | 1    | 0.5  | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C14 | 1       | 0    | 0    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C15 | 1       | 0    | 0    | 1    | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C16 | 1       | 0    | 0    | 0.5  | 1      | 0    | 1   | 0   | 0    | 1     | 0        |
|            | C17 | 0       | 1    | 1    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
|            | C18 | 0       | 1    | 0.5  | 1    | 1      | 0.75 | 0   | 0   | 0    | 1     | 0        |
|            | C19 | 0       | 1    | 1    | 0.5  | 1      | 0.5  | 0   | 0   | 0    | 1     | 0        |
|            | C20 | 0       | 1    | 0    | 1    | 1      | 1    | 0   | 0   | 0    | 1     | 0        |
| FFG        | C21 | 0       | 0    | 1    | 1    | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C22 | 0       | 0    | 0.5  | 1    | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C23 | 0       | 0    | 1    | 0.5  | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C24 | 0       | 0    | 0.67 | 0.67 | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C25 | 0       | 0    | 0    | 1    | 0      | 0    | 1   | 0   | 0    | 0     | 0        |
|            | C26 | 0       | 0    | 0    | 0.5  | 0      | 0    | 1   | 0   | 0    | 0     | 0        |

|            |     | Mission |      |     |     |        |      |     |     |      |       |          |
|------------|-----|---------|------|-----|-----|--------|------|-----|-----|------|-------|----------|
| Ship Class | CMC | AD      | TBMD | ASW | SUW | Strike | NSFS | MIO | MCM | Mine | Intel | SubIntel |
| LCS        | C27 | 0       | 0    | 1   | 0   | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C28 | 0       | 0    | 0   | 1   | 0      | 0    | 1   | 0   | 0    | 0     | 0        |
|            | C29 | 0       | 0    | 0   | 0.5 | 0      | 0    | 1   | 0   | 0    | 0     | 0        |
|            | C30 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 1   | 0    | 0     | 0        |
| SSN        | C31 | 0       | 0    | 1   | 1   | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C32 | 0       | 0    | 1   | 0.5 | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C33 | 0       | 0    | 0.5 | 1   | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C34 | 0       | 0    | 1   | 0   | 0      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C35 | 0       | 0    | 0   | 0   | 1      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C36 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 0   | 1    | 0     | 0.5      |
|            | C37 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 0   | 1    | 0     | 1        |
| SSGN       | C38 | 0       | 0    | 0   | 0   | 1      | 0    | 0   | 0   | 0    | 0     | 0        |
|            | C39 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 0   | 1    | 0     | 0.5      |
|            | C40 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 0   | 0.5  | 0     | 1        |
| MCM        | C41 | 0       | 0    | 0   | 0   | 0      | 0    | 0   | 1   | 0    | 0     | 0        |

## APPENDIX D. FULL MISSION SET

The following table displays the full mission set defined in our scenario. We assign a mission identifier and an include flag. As defined in Chapter III, a mission is a mission type required in a region for a given time period with a defined value and prerequisite missions. For example, mission m15, included in the scenario, is a NSFS mission required in region r4 on days five through eight. Mission m15 has a value of 5 and requires AD as a prerequisite. Note that m80 is inserted in region r2 for the second and succeeding scenario runs.

| Mission | Include | Type   | Region | Start Day | End Day | Value | Requires |     |
|---------|---------|--------|--------|-----------|---------|-------|----------|-----|
| m1      | x       | MIO    | r1     | 1         | 4       | 9     | AD       |     |
| m2      | x       | AD     | r1     | 1         | 4       | 7     |          |     |
| m3      | x       | ASW    | r1     | 1         | 4       | 8     | AD       | SUW |
| m4      | x       | Intel  | r1     | 1         | 4       | 7     |          |     |
| m5      | x       | TBMD   | r2     | 1         | 15      | 20    | AD       |     |
| m80     | x       | AD     | r2     | 1         | 15      | 20    |          |     |
| m6      | x       | MIO    | r3     | 1         | 4       | 5     | AD       |     |
| m7      | x       | AD     | r3     | 1         | 15      | 3     |          |     |
| m8      | x       | ASW    | r3     | 1         | 4       | 4     | AD       |     |
| m9      | x       | Intel  | r3     | 1         | 15      | 3     |          |     |
| m10     | x       | MIO    | r4     | 1         | 4       | 7     | AD       |     |
| m11     | x       | AD     | r4     | 1         | 15      | 5     |          |     |
| m12     | x       | ASW    | r4     | 1         | 4       | 6     | SUW      |     |
| m13     | x       | Intel  | r4     | 1         | 15      | 5     |          |     |
| m14     | x       | Strike | r4     | 5         | 11      | 7     | AD       |     |
| m15     | x       | NSFS   | r4     | 5         | 8       | 5     | AD       |     |
| m16     | x       | SUW    | r4     | 5         | 11      | 5     | AD       |     |
| m17     | x       | MIO    | r4     | 12        | 15      | 3     | AD       |     |
| m18     | x       | ASW    | r4     | 12        | 15      | 3     | SUW      |     |
| m19     | x       | MIO    | r5     | 1         | 4       | 5     | AD       |     |
| m20     | x       | AD     | r5     | 1         | 15      | 3     |          |     |
| m21     | x       | ASW    | r5     | 1         | 4       | 4     | SUW      |     |
| m22     | x       | Intel  | r5     | 1         | 15      | 3     |          |     |
| m23     | x       | Strike | r5     | 5         | 11      | 15    | AD       |     |
| m24     | x       | NSFS   | r5     | 5         | 8       | 7     | AD       |     |
| m25     | x       | SUW    | r5     | 5         | 11      | 7     | AD       |     |
| m26     | x       | MIO    | r5     | 12        | 15      | 5     | AD       |     |
| m27     | x       | ASW    | r5     | 12        | 15      | 5     | SUW      |     |
| m28     | x       | MIO    | r7     | 1         | 4       | 9     | AD       |     |
| m29     | x       | AD     | r7     | 1         | 15      | 7     |          |     |
| m30     | x       | ASW    | r7     | 1         | 15      | 8     | AD       | SUW |

| Mission | Include | Type     | Region | Start Day | End Day | Value | Requires |     |
|---------|---------|----------|--------|-----------|---------|-------|----------|-----|
| m31     | x       | Intel    | r7     | 1         | 15      | 7     |          |     |
| m32     | x       | Strike   | r7     | 5         | 11      | 15    | AD       |     |
| m33     | x       | NSFS     | r7     | 5         | 8       | 7     | AD       |     |
| m34     | x       | SUW      | r7     | 5         | 11      | 7     | AD       |     |
| m35     | x       | MIO      | r7     | 12        | 15      | 5     | AD       |     |
| m36     | x       | ASW      | r7     | 12        | 15      | 5     | SUW      |     |
| m37     | x       | MIO      | r8     | 1         | 4       | 5     | AD       |     |
| m38     | x       | AD       | r8     | 1         | 15      | 3     |          |     |
| m39     | x       | ASW      | r8     | 1         | 4       | 4     | SUW      |     |
| m40     | x       | Intel    | r8     | 1         | 15      | 3     |          |     |
| m41     | x       | Strike   | r8     | 5         | 11      | 5     | AD       |     |
| m42     | x       | NSFS     | r8     | 5         | 8       | 3     | AD       |     |
| m43     | x       | SUW      | r8     | 5         | 11      | 3     | AD       |     |
| m44     | x       | MIO      | r9     | 1         | 4       | 7     | AD       |     |
| m45     | x       | AD       | r9     | 1         | 15      | 5     |          |     |
| m46     | x       | ASW      | r9     | 1         | 4       | 6     | SUW      |     |
| m47     | x       | Intel    | r9     | 1         | 15      | 5     |          |     |
| m48     | x       | Strike   | r9     | 5         | 11      | 5     | AD       |     |
| m49     | x       | NSFS     | r9     | 5         | 8       | 3     | AD       |     |
| m50     | x       | SUW      | r9     | 5         | 11      | 3     | AD       |     |
| m51     | x       | MIO      | r10    | 1         | 4       | 5     | AD       |     |
| m52     | x       | AD       | r10    | 1         | 15      | 3     |          |     |
| m53     | x       | ASW      | r10    | 1         | 4       | 4     | SUW      |     |
| m54     | x       | Intel    | r10    | 1         | 15      | 3     |          |     |
| m55     | x       | Strike   | r10    | 5         | 11      | 7     | AD       |     |
| m56     | x       | NSFS     | r10    | 5         | 8       | 5     | AD       |     |
| m57     | x       | SUW      | r10    | 5         | 11      | 5     | AD       |     |
| m58     | x       | MIO      | r10    | 12        | 15      | 3     | AD       |     |
| m59     | x       | ASW      | r10    | 12        | 15      | 3     | SUW      |     |
| m60     | x       | MIO      | r11    | 1         | 4       | 7     | AD       |     |
| m61     | x       | AD       | r11    | 1         | 15      | 5     |          |     |
| m62     | x       | ASW      | r11    | 1         | 4       | 6     | SUW      |     |
| m63     | x       | Intel    | r11    | 1         | 15      | 5     |          |     |
| m64     | x       | Strike   | r11    | 5         | 11      | 7     | AD       |     |
| m65     | x       | NSFS     | r11    | 5         | 8       | 5     | AD       |     |
| m66     | x       | SUW      | r11    | 5         | 11      | 5     | AD       |     |
| m67     | x       | MIO      | r11    | 12        | 15      | 3     | AD       |     |
| m68     | x       | ASW      | r11    | 12        | 15      | 3     | SUW      |     |
| m69     | x       | ASW      | r12    | 1         | 15      | 20    |          |     |
| m70     | x       | MIO      | r13    | 1         | 4       | 9     | AD       |     |
| m71     | x       | AD       | r13    | 1         | 15      | 7     |          |     |
| m72     | x       | ASW      | r13    | 1         | 15      | 8     | AD       | SUW |
| m73     | x       | Intel    | r13    | 1         | 15      | 7     |          |     |
| m74     | x       | Strike   | r13    | 5         | 11      | 15    | AD       |     |
| m75     | x       | NSFS     | r13    | 5         | 8       | 7     | AD       |     |
| m76     | x       | SUW      | r13    | 5         | 11      | 7     | AD       |     |
| m77     | x       | MIO      | r13    | 12        | 15      | 5     | AD       |     |
| m78     | x       | ASW      | r13    | 12        | 15      | 5     | SUW      |     |
| m79     | x       | SubIntel | r16    | 1         | 15      | 20    |          |     |

## APPENDIX E. EMPLOYMENT SCHEDULE SET—INITIAL RUN

The following table displays the full NMP-produced set of optimal employment schedules for the first run of our scenario. The first run includes no pre-assigned AD in region r2 and 3 max stall days. For each ship, the schedule number is listed, as well as the employment data for each day of the planning horizon. Day, region, CMC, and mission types are listed. Note that only those mission types which accrue value are listed. In many instances, this results in the display of a subset of the listed CMC. For full description of the CMC, refer to Appendix C.

| COMBAT SHIP EMPLOYMENT SCHEDULE |        |          |    |       |        |       |       |  |
|---------------------------------|--------|----------|----|-------|--------|-------|-------|--|
| CG61                            | p3     |          |    |       |        |       |       |  |
| d1                              | r2     | C5       | AD |       |        |       |       |  |
| d2                              | r2     | C7       |    |       |        |       |       |  |
| d3                              | r2     | C7       |    |       |        |       |       |  |
| d4                              | r3     | C5       | AD | MIO   | Intel  |       |       |  |
| d5                              | r3     | C5       | AD | Intel |        |       |       |  |
| d6                              | r3     | C5       | AD | Intel |        |       |       |  |
| d7                              | r4     | C1       | AD | SUW   | Strike | NSFS  | Intel |  |
| d8                              | r4     | C1       | AD | SUW   | Strike | NSFS  | Intel |  |
| d9                              | r4     | C5       | AD | SUW   | Strike | Intel |       |  |
| d10                             | r5     | C1       | AD | SUW   | Strike | Intel |       |  |
| d11                             | r5     | C5       | AD | SUW   | Strike | Intel |       |  |
| d12                             | r5     | C5       | AD | SUW   | MIO    | Intel |       |  |
| d14                             | r7     | C1       | AD | ASW   | SUW    | Intel |       |  |
| d15                             | r4     | C1       | AD | ASW   | SUW    | Intel |       |  |
|                                 |        |          |    |       |        |       |       |  |
| CG66                            | p60800 |          |    |       |        |       |       |  |
| d1                              | r13    | C5       | AD | SUW   | MIO    | Intel |       |  |
| d2                              | r13    | C5       | AD | SUW   | MIO    | Intel |       |  |
| d3                              | r13    | C5       | AD | SUW   | MIO    | Intel |       |  |
| d4                              | r15    | INACTIVE |    |       |        |       |       |  |
| d7                              | r1     | INACTIVE |    |       |        |       |       |  |
| d8                              | r2     | C8       |    |       |        |       |       |  |
| d9                              | r2     | C8       |    |       |        |       |       |  |
| d10                             | r2     | C8       |    |       |        |       |       |  |
| d11                             | r3     | C5       | AD | Intel |        |       |       |  |
| d12                             | r3     | C2       | AD | Intel |        |       |       |  |
| d13                             | r3     | C5       | AD | Intel |        |       |       |  |
| d14                             | r4     | C5       | AD | SUW   | MIO    | Intel |       |  |
| d15                             | r7     | C5       | AD | SUW   | MIO    | Intel |       |  |

|       |         |     |     |       |        |        |       |       |
|-------|---------|-----|-----|-------|--------|--------|-------|-------|
| CG72  | p83337  |     |     |       |        |        |       |       |
| d4    | r7      | C6  | AD  | MIO   | Intel  |        |       |       |
| d5    | r7      | C3  | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6    | r7      | C3  | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8    | r8      | C3  | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9    | r8      | C6  | AD  | SUW   | Strike | Intel  |       |       |
| d10   | r8      | C3  | AD  | SUW   | Strike | Intel  |       |       |
| d11   | r9      | C6  | AD  | SUW   | Strike | Intel  |       |       |
| d12   | r9      | C3  | AD  | Intel |        |        |       |       |
| d13   | r10     | C9  | ASW | SUW   | Intel  |        |       |       |
| d14   | r10     | C9  | ASW | SUW   | Intel  |        |       |       |
| d15   | r10     | C9  | ASW | SUW   | Intel  |        |       |       |
|       |         |     |     |       |        |        |       |       |
| CG58  | p125012 |     |     |       |        |        |       |       |
| d7    | r10     | C4  | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8    | r10     | C4  | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9    | r10     | C4  | AD  | SUW   | Strike | Intel  |       |       |
| d11   | r11     | C4  | AD  | SUW   | Strike | Intel  |       |       |
| d12   | r11     | C5  | AD  | MIO   | Intel  |        |       |       |
| d13   | r13     | C5  | AD  | SUW   | MIO    | Intel  |       |       |
| d14   | r11     | C5  | AD  | MIO   | Intel  |        |       |       |
| d15   | r11     | C5  | AD  | MIO   | Intel  |        |       |       |
|       |         |     |     |       |        |        |       |       |
| DDG53 | p166670 |     |     |       |        |        |       |       |
| d1    | r1      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d2    | r1      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d3    | r1      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d4    | r2      | C17 |     |       |        |        |       |       |
| d5    | r2      | C17 |     |       |        |        |       |       |
| d6    | r2      | C17 |     |       |        |        |       |       |
| d7    | r3      | C11 | AD  | Intel |        |        |       |       |
| d8    | r3      | C15 | AD  | Intel |        |        |       |       |
| d9    | r3      | C15 | AD  | Intel |        |        |       |       |
| d10   | r4      | C11 | AD  | SUW   | Strike | Intel  |       |       |
| d11   | r4      | C11 | AD  | SUW   | Strike | Intel  |       |       |
| d12   | r4      | C11 | AD  | ASW   | SUW    | Intel  |       |       |
| d13   | r5      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d14   | r5      | C15 | AD  | MIO   | Intel  |        |       |       |
| d15   | r8      | C11 | AD  | Intel |        |        |       |       |
|       |         |     |     |       |        |        |       |       |
| DDG54 | p208336 |     |     |       |        |        |       |       |
| d1    | r4      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d2    | r4      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d3    | r4      | C15 | AD  | SUW   | MIO    | Intel  |       |       |
| d4    | r5      | C11 | AD  | ASW   | SUW    | Intel  |       |       |
| d5    | r5      | C11 | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6    | r5      | C11 | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8    | r7      | C11 | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d9    | r7      | C15 | AD  | SUW   | Strike | Intel  |       |       |
| d11   | r8      | C11 | AD  | SUW   | Strike | Intel  |       |       |
| d12   | r8      | C15 | AD  | Intel |        |        |       |       |
| d13   | r9      | C11 | AD  | Intel |        |        |       |       |
| d14   | r9      | C15 | AD  | Intel |        |        |       |       |
| d15   | r9      | C15 | AD  | Intel |        |        |       |       |

|        |         |          |     |       |        |        |       |       |
|--------|---------|----------|-----|-------|--------|--------|-------|-------|
| DDG86  | p250039 |          |     |       |        |        |       |       |
| d1     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d2     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d3     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d4     | r10     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d5     | r10     | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6     | r10     | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8     | r11     | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9     | r11     | INACTIVE |     |       |        |        |       |       |
| d10    | r12     | C12      | ASW |       |        |        |       |       |
| d12    | r15     | INACTIVE |     |       |        |        |       |       |
| d13    | r13     | C18      | ASW | SUW   | Intel  |        |       |       |
| d14    | r13     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d15    | r13     | C12      | AD  | ASW   | SUW    | Intel  |       |       |
|        |         |          |     |       |        |        |       |       |
| DDG90  | p291685 |          |     |       |        |        |       |       |
| d1     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d2     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d3     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d5     | r8      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6     | r8      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d7     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9     | r9      | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d10    | r10     | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d11    | r10     | C12      | AD  | SUW   | Strike | Intel  |       |       |
| d12    | r12     | INACTIVE |     |       |        |        |       |       |
| d13    | r10     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d14    | r10     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d15    | r10     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
|        |         |          |     |       |        |        |       |       |
| DDG100 | p373892 |          |     |       |        |        |       |       |
| d4     | r5      | C16      | AD  | SUW   | MIO    | Intel  |       |       |
| d5     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8     | r7      | C13      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d9     | r7      | C13      | AD  | ASW   | SUW    | Strike | Intel |       |
| d10    | r7      | C13      | AD  | SUW   | Strike | Intel  |       |       |
| d12    | r8      | C16      | AD  | Intel |        |        |       |       |
| d13    | r8      | C13      | AD  | Intel |        |        |       |       |
| d14    | r8      | C13      | AD  | Intel |        |        |       |       |
| d15    | r5      | C16      | AD  | SUW   | MIO    | Intel  |       |       |
|        |         |          |     |       |        |        |       |       |
| DDG80  | p390587 |          |     |       |        |        |       |       |
| d4     | r13     | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d5     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d6     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d7     | r15     | INACTIVE |     |       |        |        |       |       |
| d10    | r1      | INACTIVE |     |       |        |        |       |       |
| d11    | r2      | C17      |     |       |        |        |       |       |
| d12    | r2      | C17      |     |       |        |        |       |       |
| d13    | r2      | C11      |     |       |        |        |       |       |
| d14    | r3      | C11      | AD  | Intel |        |        |       |       |
| d15    | r2      | C15      | AD  |       |        |        |       |       |

|        |         |          |      |     |        |        |       |  |
|--------|---------|----------|------|-----|--------|--------|-------|--|
| DDG104 | p416672 |          |      |     |        |        |       |  |
| d4     | r4      | C15      | AD   | SUW | MIO    | Intel  |       |  |
| d5     | r4      | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d6     | r4      | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d7     | r5      | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d8     | r5      | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d9     | r5      | C11      | AD   | SUW | Strike | Intel  |       |  |
| d11    | r7      | C11      | AD   | ASW | SUW    | Strike | Intel |  |
| d12    | r7      | C11      | AD   | ASW | SUW    | Intel  |       |  |
| d13    | r7      | C11      | AD   | ASW | SUW    | Intel  |       |  |
| d14    | r2      | INACTIVE |      |     |        |        |       |  |
| d15    | r2      | C17      | TBMD |     |        |        |       |  |
|        |         |          |      |     |        |        |       |  |
| DDG97  | p458415 |          |      |     |        |        |       |  |
| d7     | r11     | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d8     | r11     | C11      | AD   | SUW | Strike | NSFS   | Intel |  |
| d9     | r11     | C15      | AD   | SUW | Strike | Intel  |       |  |
| d10    | r13     | C11      | AD   | ASW | SUW    | Strike | Intel |  |
| d11    | r13     | C11      | AD   | ASW | SUW    | Strike | Intel |  |
| d12    | r13     | C11      | AD   | ASW | SUW    | Intel  |       |  |
| d13    | r11     | C11      | AD   | ASW | SUW    | Intel  |       |  |
| d14    | r13     | C11      | AD   | ASW | SUW    | Intel  |       |  |
| d15    | r13     | C17      | ASW  | SUW | Intel  |        |       |  |
|        |         |          |      |     |        |        |       |  |
| FFG48  | p500099 |          |      |     |        |        |       |  |
| d4     | r10     | C21      | ASW  | SUW |        |        |       |  |
| d5     | r10     | C25      | SUW  |     |        |        |       |  |
| d6     | r10     | C25      | SUW  |     |        |        |       |  |
| d8     | r11     | INACTIVE |      |     |        |        |       |  |
| d9     | r11     | C21      | SUW  |     |        |        |       |  |
| d10    | r13     | INACTIVE |      |     |        |        |       |  |
| d11    | r13     | INACTIVE |      |     |        |        |       |  |
| d12    | r15     | INACTIVE |      |     |        |        |       |  |
| d13    | r13     | C21      | ASW  | SUW |        |        |       |  |
| d14    | r13     | C21      | ASW  | SUW |        |        |       |  |
| d15    | r13     | C21      | ASW  | SUW |        |        |       |  |
|        |         |          |      |     |        |        |       |  |
| FFG52  | p541686 |          |      |     |        |        |       |  |
| d4     | r11     | C22      | ASW  | SUW |        |        |       |  |
| d5     | r11     | INACTIVE |      |     |        |        |       |  |
| d6     | r11     | INACTIVE |      |     |        |        |       |  |
| d7     | r12     | C22      | ASW  |     |        |        |       |  |
| d8     | r12     | C22      | ASW  |     |        |        |       |  |
| d9     | r12     | C22      | ASW  |     |        |        |       |  |
| d11    | r13     | C22      | ASW  | SUW |        |        |       |  |
| d12    | r13     | C25      | SUW  | MIO |        |        |       |  |
| d13    | r11     | C25      | SUW  | MIO |        |        |       |  |
| d14    | r13     | C22      | ASW  | SUW |        |        |       |  |
| d15    | r13     | C25      | SUW  | MIO |        |        |       |  |



|        |         |          |          |     |  |  |  |  |
|--------|---------|----------|----------|-----|--|--|--|--|
| FFG47  | p583365 |          |          |     |  |  |  |  |
| d7     | r8      | INACTIVE |          |     |  |  |  |  |
| d8     | r8      | C26      | SUW      |     |  |  |  |  |
| d9     | r8      | C26      | SUW      |     |  |  |  |  |
| d10    | r5      | INACTIVE |          |     |  |  |  |  |
| d11    | r5      | INACTIVE |          |     |  |  |  |  |
| d12    | r5      | INACTIVE |          |     |  |  |  |  |
| d14    | r7      | C26      | SUW      | MIO |  |  |  |  |
| d15    | r7      | INACTIVE |          |     |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN752 | p646856 |          |          |     |  |  |  |  |
| d1     | r12     | C31      | ASW      |     |  |  |  |  |
| d2     | r12     | C31      | ASW      |     |  |  |  |  |
| d3     | r12     | C31      | ASW      |     |  |  |  |  |
| d5     | r13     | C31      | ASW      | SUW |  |  |  |  |
| d6     | r13     | C31      | ASW      | SUW |  |  |  |  |
| d7     | r15     | INACTIVE |          |     |  |  |  |  |
| d9     | r16     | C37      | SubIntel |     |  |  |  |  |
| d12    | r2      | INACTIVE |          |     |  |  |  |  |
| d13    | r4      | C31      | ASW      | SUW |  |  |  |  |
| d14    | r4      | C31      | ASW      | SUW |  |  |  |  |
| d15    | r7      | C31      | ASW      | SUW |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN718 | p666683 |          |          |     |  |  |  |  |
| d6     | r7      | C34      |          |     |  |  |  |  |
| d8     | r8      | INACTIVE |          |     |  |  |  |  |
| d10    | r10     | INACTIVE |          |     |  |  |  |  |
| d11    | r12     | C34      | ASW      |     |  |  |  |  |
| d13    | r15     | INACTIVE |          |     |  |  |  |  |
| d15    | r16     | C37      | SubIntel |     |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN717 | p719267 |          |          |     |  |  |  |  |
| d1     | r16     | C37      | SubIntel |     |  |  |  |  |
| d2     | r16     | C37      | SubIntel |     |  |  |  |  |
| d3     | r16     | C37      | SubIntel |     |  |  |  |  |
| d6     | r1      | INACTIVE |          |     |  |  |  |  |
| d7     | r3      | INACTIVE |          |     |  |  |  |  |
| d8     | r4      | C33      | SUW      |     |  |  |  |  |
| d9     | r4      | C33      | SUW      |     |  |  |  |  |
| d10    | r4      | C33      | SUW      |     |  |  |  |  |
| d11    | r5      | C33      | SUW      |     |  |  |  |  |
| d12    | r5      | C33      | ASW      | SUW |  |  |  |  |
| d13    | r5      | C33      | ASW      | SUW |  |  |  |  |
| d14    | r4      | INACTIVE |          |     |  |  |  |  |
| d15    | r5      | C33      | ASW      | SUW |  |  |  |  |

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## APPENDIX F. EMPLOYMENT SCHEDULE SET—FOURTH RUN

The following table displays the full NMP-produced set of optimal employment schedules for the fourth run of our scenario. The table includes the explicitly assigned AD mission in region r2 and 15 max stall days. As in Appendix E, each ship and its schedule number are listed, as well as the employment data for each day of the planning horizon. Day, region, CMC, and mission types are listed. Again note that only those mission types which accrue value are listed. For full description of the CMC, refer to Appendix C.

| COMBAT SHIP EMPLOYMENT SCHEDULE |        |          |      |     |     |        |       |       |  |
|---------------------------------|--------|----------|------|-----|-----|--------|-------|-------|--|
| CG61                            | p4     |          |      |     |     |        |       |       |  |
| d1                              | r2     | C5       | AD   |     |     |        |       |       |  |
| d2                              | r2     | C7       | TBMD |     |     |        |       |       |  |
| d3                              | r2     | C1       | AD   |     |     |        |       |       |  |
| d4                              | r2     | C5       | AD   |     |     |        |       |       |  |
| d5                              | r2     | C1       | AD   |     |     |        |       |       |  |
| d6                              | r2     | C7       | TBMD |     |     |        |       |       |  |
| d7                              | r2     | C7       | TBMD |     |     |        |       |       |  |
| d8                              | r2     | C1       | AD   |     |     |        |       |       |  |
| d9                              | r2     | C1       | AD   |     |     |        |       |       |  |
| d10                             | r2     | C7       | TBMD |     |     |        |       |       |  |
| d11                             | r2     | C7       | TBMD |     |     |        |       |       |  |
| d12                             | r2     | C7       | TBMD |     |     |        |       |       |  |
| d13                             | r2     | C7       | TBMD |     |     |        |       |       |  |
| d14                             | r2     | C1       | AD   |     |     |        |       |       |  |
| d15                             | r7     | C5       | AD   | SUW | MIO | Intel  |       |       |  |
|                                 |        |          |      |     |     |        |       |       |  |
| CG66                            | p41685 |          |      |     |     |        |       |       |  |
| d1                              | r13    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d2                              | r13    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d3                              | r13    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d4                              | r13    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d5                              | r13    | C2       | AD   | ASW | SUW | Strike | NSFS  | Intel |  |
| d6                              | r13    | C2       | AD   | ASW | SUW | Strike | NSFS  | Intel |  |
| d7                              | r13    | C2       | AD   | ASW | SUW | Strike | NSFS  | Intel |  |
| d8                              | r13    | INACTIVE |      |     |     |        |       |       |  |
| d9                              | r13    | C2       | AD   | ASW | SUW | Strike | Intel |       |  |
| d10                             | r13    | C2       | AD   | ASW | SUW | Strike | Intel |       |  |
| d11                             | r13    | C2       | AD   | ASW | SUW | Strike | Intel |       |  |
| d12                             | r13    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d13                             | r11    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d14                             | r11    | C5       | AD   | SUW | MIO | Intel  |       |       |  |
| d15                             | r11    | C5       | AD   | SUW | MIO | Intel  |       |       |  |

|       |         |          |      |       |        |        |       |       |
|-------|---------|----------|------|-------|--------|--------|-------|-------|
| CG72  | p83343  |          |      |       |        |        |       |       |
| d4    | r7      | C3       | AD   | ASW   | SUW    | Intel  |       |       |
| d5    | r7      | C3       | AD   | ASW   | SUW    | Strike | NSFS  | Intel |
| d6    | r7      | C3       | AD   | ASW   | SUW    | Strike | NSFS  | Intel |
| d7    | r7      | C3       | AD   | ASW   | SUW    | Strike | NSFS  | Intel |
| d8    | r7      | C3       | AD   | ASW   | SUW    | Strike | NSFS  | Intel |
| d9    | r7      | C3       | AD   | ASW   | SUW    | Strike | Intel |       |
| d10   | r7      | C6       | AD   | SUW   | Strike | Intel  |       |       |
| d11   | r7      | C6       | AD   | SUW   | Strike | Intel  |       |       |
| d12   | r7      | C3       | AD   | ASW   | SUW    | Intel  |       |       |
| d13   | r7      | C9       | ASW  | SUW   | Intel  |        |       |       |
| d14   | r4      | C6       | AD   | MIO   | Intel  |        |       |       |
| d15   | r5      | C6       | AD   | SUW   | MIO    | Intel  |       |       |
| CG58  | p125002 |          |      |       |        |        |       |       |
| d7    | r10     | C4       | AD   | SUW   | Strike | NSFS   | Intel |       |
| d8    | r10     | C4       | AD   | SUW   | Strike | NSFS   | Intel |       |
| d9    | r10     | C4       | AD   | SUW   | Strike | Intel  |       |       |
| d10   | r10     | C5       | AD   | SUW   | Strike | Intel  |       |       |
| d11   | r10     | C4       | AD   | SUW   | Strike | Intel  |       |       |
| d12   | r10     | C5       | AD   | MIO   | Intel  |        |       |       |
| d13   | r10     | C5       | AD   | MIO   | Intel  |        |       |       |
| d14   | r10     | C5       | AD   | MIO   | Intel  |        |       |       |
| d15   | r10     | C5       | AD   | MIO   | Intel  |        |       |       |
| DDG53 | p184524 |          |      |       |        |        |       |       |
| d1    | r1      | C15      | AD   | SUW   | MIO    | Intel  |       |       |
| d2    | r1      | C15      | AD   | SUW   | MIO    | Intel  |       |       |
| d3    | r1      | C15      | AD   | SUW   | MIO    | Intel  |       |       |
| d4    | r1      | C15      | AD   | MIO   | Intel  |        |       |       |
| d5    | r2      | C17      | TBMD |       |        |        |       |       |
| d6    | r2      | C17      | TBMD |       |        |        |       |       |
| d7    | r2      | C17      | TBMD |       |        |        |       |       |
| d8    | r2      | INACTIVE |      |       |        |        |       |       |
| d9    | r2      | C17      | TBMD |       |        |        |       |       |
| d10   | r2      | C17      | TBMD |       |        |        |       |       |
| d11   | r2      | C17      | TBMD |       |        |        |       |       |
| d12   | r2      | INACTIVE |      |       |        |        |       |       |
| d13   | r2      | C17      | TBMD |       |        |        |       |       |
| d14   | r3      | C15      | AD   | Intel |        |        |       |       |
| d15   | r2      | C17      | TBMD |       |        |        |       |       |
| DDG54 | p208338 |          |      |       |        |        |       |       |
| d1    | r2      | C17      | TBMD |       |        |        |       |       |
| d2    | r2      | C11      | AD   |       |        |        |       |       |
| d3    | r2      | C17      | TBMD |       |        |        |       |       |
| d4    | r2      | C17      | TBMD |       |        |        |       |       |
| d5    | r2      | C17      | TBMD |       |        |        |       |       |
| d6    | r2      | C11      | AD   |       |        |        |       |       |
| d7    | r2      | C11      | AD   |       |        |        |       |       |
| d8    | r2      | C17      | TBMD |       |        |        |       |       |
| d9    | r2      | C17      | TBMD |       |        |        |       |       |
| d10   | r2      | C11      | AD   |       |        |        |       |       |
| d11   | r2      | C15      | AD   |       |        |        |       |       |
| d12   | r2      | C15      | AD   |       |        |        |       |       |
| d13   | r2      | C11      | AD   |       |        |        |       |       |
| d14   | r2      | C17      | TBMD |       |        |        |       |       |
| d15   | r4      | C11      | AD   | ASW   | SUW    | Intel  |       |       |

|        |         |          |     |       |        |        |       |       |
|--------|---------|----------|-----|-------|--------|--------|-------|-------|
| DDG86  | p250003 |          |     |       |        |        |       |       |
| d1     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d2     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d3     | r9      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d4     | r9      | C15      | AD  | MIO   | Intel  |        |       |       |
| d5     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d7     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8     | r9      | C12      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9     | r9      | C12      | AD  | SUW   | Strike | Intel  |       |       |
| d10    | r9      | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d11    | r9      | C12      | AD  | SUW   | Strike | Intel  |       |       |
| d12    | r9      | C15      | AD  | Intel |        |        |       |       |
| d13    | r9      | C15      | AD  | Intel |        |        |       |       |
| d14    | r9      | C15      | AD  | Intel |        |        |       |       |
| d15    | r9      | C12      | AD  | Intel |        |        |       |       |
| DDG90  | p291671 |          |     |       |        |        |       |       |
| d1     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d2     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d3     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d4     | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d5     | r7      | C12      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d6     | r7      | C12      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d7     | r7      | C12      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d8     | r7      | C12      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d9     | r7      | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d10    | r7      | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d11    | r7      | C15      | AD  | SUW   | Strike | Intel  |       |       |
| d12    | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d13    | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d14    | r7      | C15      | AD  | SUW   | MIO    | Intel  |       |       |
| d15    | r2      | C12      | AD  |       |        |        |       |       |
| DDG100 | p361136 |          |     |       |        |        |       |       |
| d4     | r5      | C16      | AD  | MIO   | Intel  |        |       |       |
| d5     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d6     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d7     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d8     | r5      | C13      | AD  | SUW   | Strike | NSFS   | Intel |       |
| d9     | r5      | C13      | AD  | SUW   | Strike | Intel  |       |       |
| d10    | r5      | C16      | AD  | SUW   | Strike | Intel  |       |       |
| d11    | r5      | C16      | AD  | SUW   | Strike | Intel  |       |       |
| d12    | r5      | C16      | AD  | SUW   | MIO    | Intel  |       |       |
| d13    | r5      | C13      | AD  | ASW   | SUW    | Intel  |       |       |
| d14    | r8      | C16      | AD  | Intel |        |        |       |       |
| d15    | r8      | C13      | AD  | Intel |        |        |       |       |
| DDG80  | p375023 |          |     |       |        |        |       |       |
| d4     | r13     | C11      | AD  | ASW   | SUW    | Intel  |       |       |
| d5     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d6     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d7     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d8     | r13     | C11      | AD  | ASW   | SUW    | Strike | NSFS  | Intel |
| d9     | r13     | C11      | AD  | ASW   | SUW    | Strike | Intel |       |
| d10    | r13     | C11      | AD  | ASW   | SUW    | Strike | Intel |       |
| d11    | r13     | INACTIVE |     |       |        |        |       |       |
| d12    | r13     | C17      | ASW | SUW   | Intel  |        |       |       |
| d13    | r11     | C17      | ASW | SUW   | Intel  |        |       |       |
| d14    | r11     | C11      | AD  | ASW   | SUW    | Intel  |       |       |
| d15    | r13     | C11      | AD  | ASW   | SUW    | Intel  |       |       |

|        |         |          |     |       |        |       |       |  |
|--------|---------|----------|-----|-------|--------|-------|-------|--|
| DDG104 | p416677 |          |     |       |        |       |       |  |
| d4     | r4      | C15      | AD  | SUW   | MIO    | Intel |       |  |
| d5     | r4      | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d6     | r4      | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d7     | r4      | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d8     | r4      | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d9     | r4      | C11      | AD  | SUW   | Strike | Intel |       |  |
| d10    | r4      | C15      | AD  | SUW   | Strike | Intel |       |  |
| d11    | r4      | C15      | AD  | SUW   | Strike | Intel |       |  |
| d12    | r4      | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d13    | r4      | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d14    | r5      | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d15    | r3      | C15      | AD  | Intel |        |       |       |  |
|        |         |          |     |       |        |       |       |  |
| DDG97  | p458354 |          |     |       |        |       |       |  |
| d7     | r11     | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d8     | r11     | C11      | AD  | SUW   | Strike | NSFS  | Intel |  |
| d9     | r11     | C15      | AD  | SUW   | Strike | Intel |       |  |
| d10    | r11     | C15      | AD  | SUW   | Strike | Intel |       |  |
| d11    | r11     | C11      | AD  | SUW   | Strike | Intel |       |  |
| d12    | r11     | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d13    | r13     | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d14    | r13     | C11      | AD  | ASW   | SUW    | Intel |       |  |
| d15    | r13     | C11      | AD  | ASW   | SUW    | Intel |       |  |
|        |         |          |     |       |        |       |       |  |
| FFG48  | p500120 |          |     |       |        |       |       |  |
| d4     | r10     | C21      | ASW | SUW   |        |       |       |  |
| d5     | r10     | INACTIVE |     |       |        |       |       |  |
| d6     | r10     | INACTIVE |     |       |        |       |       |  |
| d7     | r10     | C21      | SUW |       |        |       |       |  |
| d8     | r10     | C21      | SUW |       |        |       |       |  |
| d9     | r12     | C21      | ASW |       |        |       |       |  |
| d10    | r12     | C21      | ASW |       |        |       |       |  |
| d11    | r12     | C21      | ASW |       |        |       |       |  |
| d12    | r12     | C21      | ASW |       |        |       |       |  |
| d13    | r12     | C21      | ASW |       |        |       |       |  |
| d14    | r12     | C21      | ASW |       |        |       |       |  |
| d15    | r12     | C21      | ASW |       |        |       |       |  |
|        |         |          |     |       |        |       |       |  |
| FFG52  | p541688 |          |     |       |        |       |       |  |
| d4     | r11     | C22      | ASW | SUW   |        |       |       |  |
| d5     | r11     | INACTIVE |     |       |        |       |       |  |
| d6     | r11     | INACTIVE |     |       |        |       |       |  |
| d7     | r11     | C25      | SUW |       |        |       |       |  |
| d8     | r11     | C22      | SUW |       |        |       |       |  |
| d9     | r11     | INACTIVE |     |       |        |       |       |  |
| d10    | r11     | C25      | SUW |       |        |       |       |  |
| d11    | r11     | INACTIVE |     |       |        |       |       |  |
| d12    | r11     | C25      | SUW | MIO   |        |       |       |  |
| d13    | r13     | C25      | SUW | MIO   |        |       |       |  |
| d14    | r13     | C25      | SUW | MIO   |        |       |       |  |
| d15    | r13     | C25      | SUW | MIO   |        |       |       |  |

|        |         |          |          |     |  |  |  |  |
|--------|---------|----------|----------|-----|--|--|--|--|
| FFG47  | p599405 |          |          |     |  |  |  |  |
| d7     | r8      | INACTIVE |          |     |  |  |  |  |
| d8     | r8      | INACTIVE |          |     |  |  |  |  |
| d9     | r8      | INACTIVE |          |     |  |  |  |  |
| d10    | r8      | INACTIVE |          |     |  |  |  |  |
| d11    | r8      | INACTIVE |          |     |  |  |  |  |
| d12    | r5      | C23      | ASW      | SUW |  |  |  |  |
| d13    | r5      | C26      | SUW      | MIO |  |  |  |  |
| d14    | r5      | C26      | SUW      | MIO |  |  |  |  |
| d15    | r5      | C23      | ASW      | SUW |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN752 | p625242 |          |          |     |  |  |  |  |
| d1     | r12     | C31      | ASW      |     |  |  |  |  |
| d2     | r12     | C31      | ASW      |     |  |  |  |  |
| d3     | r12     | C31      | ASW      |     |  |  |  |  |
| d4     | r12     | C31      | ASW      |     |  |  |  |  |
| d5     | r12     | C31      | ASW      |     |  |  |  |  |
| d6     | r12     | C31      | ASW      |     |  |  |  |  |
| d7     | r12     | C31      | ASW      |     |  |  |  |  |
| d8     | r12     | C31      | ASW      |     |  |  |  |  |
| d10    | r15     | INACTIVE |          |     |  |  |  |  |
| d11    | r11     | INACTIVE |          |     |  |  |  |  |
| d12    | r13     | C31      | ASW      | SUW |  |  |  |  |
| d13    | r13     | C31      | ASW      | SUW |  |  |  |  |
| d14    | r13     | C31      | ASW      | SUW |  |  |  |  |
| d15    | r11     | C31      | ASW      | SUW |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN718 | p666673 |          |          |     |  |  |  |  |
| d6     | r7      | C34      | ASW      |     |  |  |  |  |
| d7     | r7      | C34      | ASW      |     |  |  |  |  |
| d8     | r7      | C34      | ASW      |     |  |  |  |  |
| d9     | r7      | C34      | ASW      |     |  |  |  |  |
| d10    | r7      | C34      | ASW      |     |  |  |  |  |
| d11    | r7      | C34      | ASW      |     |  |  |  |  |
| d12    | r7      | C34      | ASW      |     |  |  |  |  |
| d13    | r7      | C34      | ASW      |     |  |  |  |  |
| d14    | r7      | C34      | ASW      |     |  |  |  |  |
| d15    | r7      | C34      | ASW      |     |  |  |  |  |
|        |         |          |          |     |  |  |  |  |
| SSN717 | p708340 |          |          |     |  |  |  |  |
| d1     | r16     | C37      | SubIntel |     |  |  |  |  |
| d2     | r16     | C37      | SubIntel |     |  |  |  |  |
| d3     | r16     | C37      | SubIntel |     |  |  |  |  |
| d4     | r16     | C37      | SubIntel |     |  |  |  |  |
| d5     | r16     | C37      | SubIntel |     |  |  |  |  |
| d6     | r16     | C37      | SubIntel |     |  |  |  |  |
| d7     | r16     | C37      | SubIntel |     |  |  |  |  |
| d8     | r16     | C37      | SubIntel |     |  |  |  |  |
| d9     | r16     | C37      | SubIntel |     |  |  |  |  |
| d10    | r16     | C37      | SubIntel |     |  |  |  |  |
| d11    | r16     | C37      | SubIntel |     |  |  |  |  |
| d12    | r16     | C37      | SubIntel |     |  |  |  |  |
| d13    | r16     | C37      | SubIntel |     |  |  |  |  |
| d14    | r16     | C37      | SubIntel |     |  |  |  |  |
| d15    | r16     | C37      | SubIntel |     |  |  |  |  |

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